3 Channel 5.5V 2A 1.5MHz DC/DC Step down PMU

Feature

- 2.7V to 5.5V Input Voltage Range
- Three Buck Converters
- Output Voltage Range: 0.6V to Vin
- Maximum Continuous Load Current:2A (3CH total output power consumption must be less than 6W)
- 180° Phases Shifted Architecture
- Fixed 1.5MHz Switching Frequency
- 100% Duty Cycle Low Dropout Operation
- <1uA Shutdown Current
- Independent Enable Control
- Internal Compensation
- Cycle-by-Cycle Current Limit
- Short Circuit Protection
- Each Channel Efficiency Up to 95%
- Auto Recovery OTP Protection
- Available in 20-pin 3mm × 3mm QFN Package

Applications

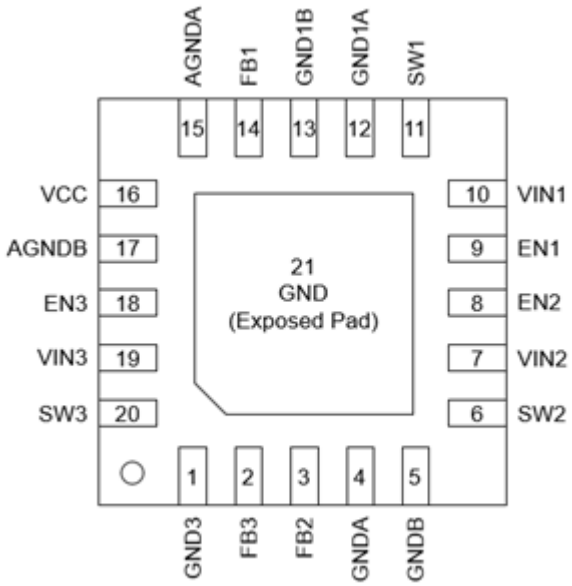
- IP Camera
- Video Door Bell
- DVR
- OTT/STB

General Description

The RY1303 is a 3-CH power management IC for applications powered by one Li-Ion battery or a DC 5V adapter. It integrates three synchronous buck regulators and can provide high efficiency output at light load and heavy load operation. The internal compensation architecture simplifies the application circuit design. Besides, the independent enable control makes the designer have the greatest flexibility to optimize timing for power sequencing purposes. The RY1303 is available in a 20 pin QFN 3×3package.

PIN Description

Pin Configuration



(QFN20-3×3)

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Pin Description

Item	Name	Function Description
1	GND3	Power ground pin of CH3.
2	FB3	Feedback input of CH3. Connect to output voltage with a resistor divider.
3	FB2	Feedback input of CH2. Connect to output voltage with a resistor divider.
4	GND2A	Power ground pin of CH2.
5	GND2B	Power ground pin of CH2.
6	SW2	Internal MOSFET switching output of CH2. Connect SW2 pin with a low pass filter circuit to obtain a stable DC output voltage.
7	VIN2	Power input pin of CH2. Recommended to use a 10uF MLCC capacitor between VIN2 pin and GND2 pin.
8	EN2	CH2 turns on/turns off control input. Don't leave this pin floating.
9	EN1	CH1 turns on/turns off control input. Don't leave this pin floating.
10	VIN1	Power input pin of CH1. Recommended to use a 10uF MLCC capacitor between VIN1 pin and GND1 pin.
11	SW1	Internal MOSFET switching output of CH1. Connect SW1 pin with a low pass filter circuit to obtain a stable DC output voltage.
12	GND1A	Power ground pin of CH1.
13	GND1B	Power ground pin of CH1.
14	FB1	Feedback input of CH1. Connect to output voltage with a resistor divider.
15	AGNDA	Analog ground pin.
16	VCC	Input supply pin for internal control circuit.
17	AGNDB	Analog ground pin.
18	EN3	CH3 turns on/turns off control input. Don't leave this pin floating.
19	VIN3	Power input pin of CH3. Recommended to use a 10uF MLCC capacitor between VIN3 pin and GND3 pin.
20	SW3	Internal MOSFET switching output of CH3. Connect SW3 pin with a low pass filter circuit to obtain a stable DC output voltage.
21	EP	The Exposed Pad must be soldered to a large PCB copper plane and connected to GND for appropriate dissipation.

Order Information

Marking	Part No.	Model	Description	Package	MOQ
1303 YYLL	70303002	RY1303	RY1303 3×Buck, 2.5-5.5V, 2.0A, 1.5MHz, VFB 0.6V, QFN20-3×3	QFN20-3×3	5000

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Absolute Maximum Ratings (Note 1)

Input Voltage (V_{VIN1}, V_{VIN2}, V_{VIN3}) ..... 0.3V to +6.5V
SW Pin Voltage (V_{SW1}, V_{SW2}, V_{SW3}) ..... 0.3V to V_{VINX}+0.3V
All Other Pins Voltage..... -0.3V to +6.5V
Ambient Temperature operating Range (T_A) ..... -40°C to +85°C
Maximum Junction Temperature (T_{Jmax}) ..... +150°C
Lead Temperature (Soldering, 10 sec) ..... +260°C
Storage Temperature Range (T_S) ..... -55°C to +150°C
QFN 3×3-20 Thermal Resistance (θJC) ..... 7.5°C/W
QFN 3×3-20 Thermal Resistance (θJA) ..... 50°C/W
QFN 3×3-20 Power Dissipation at TA=25°C (PDmax) 2.5W
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired

Electrical Characteristics (Note 2) (Note 3)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Supply Voltage						
Input Voltage	VINx		2.5		5.5	V
Control Circuit Input Voltage	VVCC		2.5		5.5	V
Buck Regulator 1, 2, 3						
Shutdown Supply Current	ISD	VEN = 0V	0.1		1	μA
Quiescent Current	IQ	Non-switching, No Load	30		80	μA
UVLO Threshold	VUVLO	VVIN Rising	1.9	2.3	2.5	V
UVLO Hysteresis	VUV-HYST			0.3		V
Output Load Current	ILOAD			2		A
Reference Voltage	VREF		0.588	0.6	0.612	V
Switching Frequency	FSW	ILOAD = 100mA	1	1.5	2	MHz
Short Frequency	FSW-SHORT	VOUT = 0V		350		KHz
PMOS Current Limit	ILIM-P		3.5			A
PMOS On-Resistance	RDS(ON)-P	ILOAD = 100mA		100		mΩ
NMOS On-Resistance	RDS(ON)-N	ILOAD = 100mA		90		mΩ
Enable Pin Input Low Voltage	VEN-L				0.4	V
Enable Pin Input High Voltage	VEN-H		2			V
Maximum Duty Cycle	DMAX		100			%
Thermal Shutdown						
Thermal Shutdown Threshold	TOTP			165		℃
Thermal Shutdown Hysteresis	THYST			30		℃

Note 2: MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.
Note 3: Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

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General Description

Feature Description

RY1303 is a highly efficient and integrated Power Management IC for Systems-on-a-Chip (SoCs), ASICs, and processors. The device incorporates 3 high-efficiency synchronous buck regulators.
Each of the buck regulators is specially designed for high-efficiency operation throughout the load range. With 1.5MHz typical switching frequency, the external L- C filter can be small and still provide very low output voltage ripple. The bucks are internally compensated to be stable with the recommended external inductors and capacitors as detailed in the application diagram. Synchronous rectification yields high efficiency for low voltage and high output currents.
Additional features include soft-start, under-voltage lockout, bypass, and current and thermal overload protection.
3 channel BUCKs are nearly identical in performance and mode of operation. They can operate in automatic mode (PWM/PFM). At very light loads, BUCKs enter PFM mode and operate with reduced switching frequency and supply current to maintain high efficiency.

Soft start

Each of BUCKs has an internal soft-start circuit that limits the in-rush current during startup. This allows the converters to gradually reach the steady-state operating point, thus reducing startup stresses and surges. During startup, the switch current limit is increased in steps. The startup time depends on the output capacitor size, load current and output voltage.

Current Limiting

A current limit feature protects the device and any external components during overload conditions. In PWM mode the current limiting is implemented by using an internal comparator that trips at current levels according to the buck capability. If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

Under Voltage Lock Out (UVLO)

The VIN voltage is monitored for a supply under voltage condition, for which the operation of the device cannot be guaranteed. The part will automatically disable PMIC. To prevent unstable operation, the UVLO has a hysteresis window. An under voltage lockout (UVLO) will disable BUCKs outputs, Once the supply voltage is above the UVLO hysteresis, the device will initiate a power-up sequence and then enter the active state.

Over Voltage Lock Out (OVLO)

The VIN voltage is monitored for a supply over voltage condition, for which the operation of the device cannot be guaranteed. The purpose of OVLO is to protect the part and all other components connected to the PMIC outputs from any damage and malfunction. Once VIN rises over about 6.5V, BUCKs will be disabled automatically. To prevent unstable operation, the OVLO has a hysteresis window. An over voltage lockout (OVLO) will force the device into the reset state, Once the supply voltage goes below the OVLO lower threshold, the device will initiate a power-up sequence and then enter the active state.

Thermal Shutdown (OTP)

The temperature of the silicon die is monitored for an over-temperature condition, for which the operation of the device cannot be guaranteed. The part will automatically be disabled if the temperature is too high. The thermal shutdown (OTP) will force the device into the reset state. In reset, all circuitry is disabled. To prevent unstable operation, the OTP has a hysteresis window of about 20°C. Once the temperature has decreased below the OTP hysteresis, the device will initiate a power-up sequence and then enter the active state. In the active state, the part will start up as if for the first time.

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Detailed Design Procedure

External Components Selection

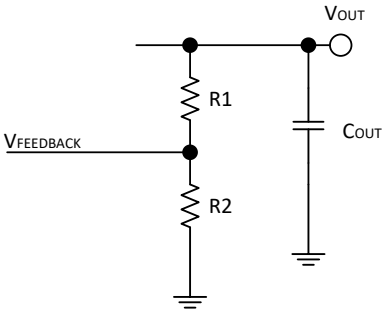
RY1303 require an input capacitor, an output capacitor and an inductor. These components are critical to the performance of the device. RY1303 are internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider.

$$V_{OUT} = V_{FEEDBACK} \times \frac{R1 + R2}{R2}$$

Select $R1$ value around 50kΩ

$$R2 = R1 \times \frac{V_{FEEDBACK}}{V_{OUT} - V_{FEEDBACK}}$$

Where $V_{FEEDBACK}$ as 0.6V



Output Inductors and Capacitors Selection

There are several design considerations related to the selection of output inductors and capacitors:

- Load transient response
- Stability
- Efficiency
- Output ripple voltage
- Over current ruggedness

The device has been optimized for use with nominal LC values as shown in the Application Diagram.

BUCK Power Supply Recommendations

RY1303 are designed to operate from input voltage supply range between 2.7V and 5.5V. This input supply must be well regulated. If the input supply is located more than a few inches, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A ceramic capacitor with a value of 10uF is a typical choice.
VIN must be connected to input capacitors as close as possible.

BUCK Inductor Selection

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the peak load current plus the ripple current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

$$I_{L(MAX)} = I_{LOAD(MAX)} + I_{RIPPLE}$$

$$= I_{LOAD(MAX)} + \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times F_S}$$

$$D = \frac{V_{OUT}}{V_{IN}}, F_S = 1.5MHz, L = 2.2uH$$

where

- $I_{L(MAX)}$: Max inductor Current
- $I_{LOAD(MAX)}$: Max load current
- I_{RIPPLE}: Peak-to-Peak inductor current

- D: Estimated duty factor
- V_{IN}: Input voltage
- V_{OUT}: Output voltage
- F_S: Switching frequency, Hertz

Recommended Method for BUCK Inductor Selection

The best way to guarantee the inductor does not saturate is to choose an inductor that has saturation current rating greater than the maximum device current limit, as specified in the Electrical Characteristics. In this case the device will prevent inductor saturation by going into current limit before the saturation level is reached.

Alternate Method for BUCK Inductor Selection

If the recommended approach cannot be used care must be taken to guarantee that the saturation current is greater than the peak inductor current:

$$I_{SAT} > IL_{PEAK}$$

$$IL_{PEAK} = I_{OUTMAX} + \frac{I_{RIPPLE}}{2}$$

$$I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{L \times F_S}$$

$$D = \frac{V_{OUT}}{V_{IN} \times EFF}$$

where

- I_{SAT}: Inductor saturation current at operating temperature
- IL_{PEAK}: Peak inductor current during worst case conditions
- I_{OUTMAX}: Maximum average inductor current
- I_{RIPPLE}: Peak-to-Peak inductor current
- V_{OUT}: Output voltage
- V_{IN}: Input voltage
- L: Inductor value in Henries at IOUTMAX
- F_S: Switching frequency, Hertz
- D: Estimated duty factor
- EFF: Estimated power supply efficiency

I_{SAT} may not be exceeded during any operation, including transients, startup, high temperature, worst case conditions, etc.

Output and Input Capacitors Characteristics

Special attention should be paid when selecting these components. The DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table.
The ceramic capacitor's actual capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1uF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X5R or X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.
Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47uF to 44uF range. Another important

consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

BUCK Output Capacitor Selection

The output capacitor of a switching converter absorbs the AC ripple current from the inductor and provides the initial response to a load transient. The ripple voltage at the output of the converter is the product of the ripple current flowing through the output capacitor and the impedance of the capacitor. The impedance of the capacitor can be dominated by capacitive, resistive, or inductive elements within the capacitor, depending on the frequency of the ripple current. Ceramic capacitors have very low ESR and remain capacitive up to high frequencies. Their inductive component can be usually neglected at the frequency ranges the switcher operates.
The output-filter capacitor smoothest out the current flow from the inductor to the load and helps maintain a steady output voltage during transient load changes. It also reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and low enough ESR to perform these functions.
Note that the output voltage ripple increases with the inductor current ripple and the Equivalent Series Resistance of the output capacitor (*ESRCOUT*).Also note that the actual value of the capacitor's *ESRCOUT* is frequency and temperature dependent, as specified by its manufacturer. The ESR should be calculated at the applicable switching frequency and ambient temperature.

$$V_{OUT-RIPPLE-PP} = \frac{I_{RIPPLE}}{8 \times F_S \times C_{OUT}}$$

where

$$I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times F_S}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

where

- $V_{OUT\text{-}RIPPLE\text{-}PP}$: estimated output voltage ripple
- I_{RIPPLE}: estimated current ripple
- D: Estimated duty factor

Output ripple can be estimated from the vector sum of the reactive (capacitance) voltage component and the real (ESR) voltage component of the output capacitor:

$$V_{OUT-RIPPLE-PP} = \sqrt{V_{ROUT}^2 + V_{COUT}^2}$$

where

$$V_{ROUT} = I_{RIPPLE} \times ESR_{COUT}$$

$$V_{COUT} = \frac{I_{RIPPLE}}{8 \times F_S \times C_{OUT}}$$

where

- $V_{OUT\text{-}RIPPLE\text{-}PP}$: estimated output ripple,
- V_{ROUT}: estimated real output ripple,
- V_{COUT}: estimated reactive output ripple.

The device is designed to be used with ceramic capacitors on the outputs of the buck regulators. The recommended

dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature. The recommended value for the output capacitors is 10µF, 6.3V with an ESR of 2mΩ or less. The output capacitors need to be mounted as close as possible to the output/ground terminals of the device.

BUCK Input Capacitor Selection

input capacitor should be located as close as possible to their corresponding VIN and GND terminals, tantalum capacitor can also be located in the proximity of the device.
The input capacitor supplies the AC switching current drawn from the switching action of the internal power MOSFETs. The input current of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle both the RMS current and the dissipated power. The input capacitor must be rated to handle this current:

$$V_{RMS\_CIN} = I_{OUT}\frac{\sqrt{V_{OUT}\times(V_{IN}-V_{OUT})}}{V_{IN}}$$

The power dissipated in the input capacitor is given by:

$$P_{D\_CIN} = I^2_{RMS\_CIN}\times R_{ESR\_CIN}$$

The device is designed to be used with ceramic capacitors on the inputs of the buck regulators. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature. The minimum recommended value for the input capacitor is 10µF with an ESR of 10mΩ or less. The input capacitors need to be mounted as close as possible to the power/ground input terminals of the device.
The input power source supplies the average current continuously. During the high side MOSFET switch on-time, however, the demanded di/dt is higher than can be typically supplied by the input power source. This delta is supplied by the input capacitor.
A simplified “worst case” assumption is that all of the high side MOSFET current is supplied by the input capacitor. This will result in conservative estimates of input ripple voltage and capacitor RMS current.
Input ripple voltage is estimated as follows:

$$V_{PPIN} = \frac{I_{OUT}\times D}{C_{IN}\times F_S} + I_{OUT}\times ESR_{CIN}$$

where

- V_{PPIN}: Estimated peak-to-peak input ripple voltage
- I_{OUT}: Output current
- C_{IN}: Input capacitor value
- ESR_{CIN}: Input capacitor ESR

This capacitor is exposed to significant RMS current, so it is important to select a capacitor with an adequate RMS current rating. Capacitor RMS current estimated as follows:

$$I_{RMSCIN} = \sqrt{D\times(I^2_{OUT} + \frac{I^2_{RIPPLE}}{12})}$$

Where

- I_{RMSCIN}: Estimated input capacitor RMS current

Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good

layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the *CIN* input capacitor, to the regulator *VIN* terminal, to the regulator *SW* terminal, to the inductor then out to the output capacitor *COUT* and load. The second loop starts from the output capacitor ground, to the regulator *GND* terminals, to the inductor and then out to *COUT* and the load. To minimize both loop areas the input capacitor should be placed as close as possible to the *VIN* terminal. Grounding for both the input and output capacitors should consist of a small localized top side plane that connects to *GND*. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The *SW* terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with a sufficient width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the *SW* terminals to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected together then routed to the *GND* pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the *FB* terminal. The feedback trace should be routed away from the *SW* pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

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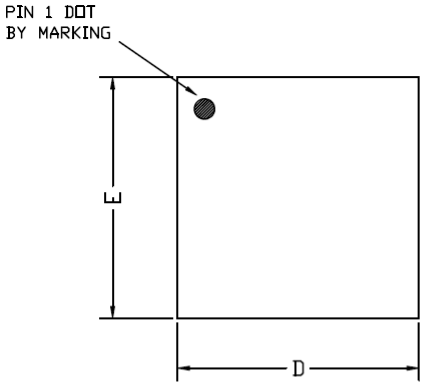
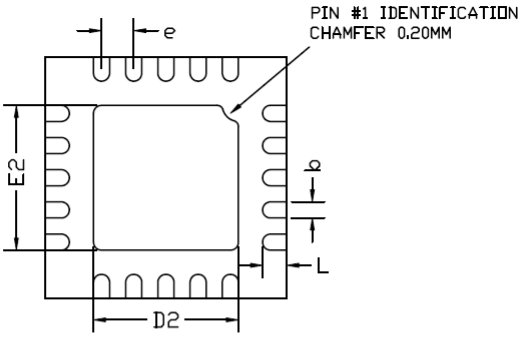
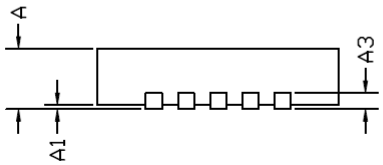
Package Description



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS(MM)			
PKG.	W)VERY VERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	–	0.05
A3	0.20 REF.		
D	2.95	3.00	3.05
E	2.95	3.00	3.05
b	0.15	0.20	0.25
L	0.25	0.30	0.35
D2	1.65	1.80	1.90
E2	1.65	1.80	1.90
e	0.40 BSC		