20W Stereo Class-D Audio Amplifier with Power Limit And Dynamic Temperature Control

Features

- Single supply voltage
  8 ~ 26V for loudspeaker driver
  Built-in LDO output 3.3V for others
- Loudspeaker power from 24V supply
  BTL Mode: 20W/CH into 8Ω @0.09% THD+N
  PBTL Mode: 40W/CH into 4Ω @0.15% THD+N
- Loudspeaker power from 13V supply
  BTL Mode: 10W/CH into 8Ω @10% THD+N
- 87% efficient Class-D operation eliminates need for heat sink
- Differential inputs
- Four selectable, fixed gain settings
- Internal oscillator
- Short-Circuit protection with auto recovery option
- Under-Voltage detection
- Over-Voltage protection
- Pop noise and click noise reduction
- Adjustable power limit function for speaker protection
- Output DC detection for speaker protection
- Filter-Free operation
- Over temperature protection with auto recovery
- Dynamic temperature control prevents chip from over heating

Applications

- TV audio
- Boom-Box
- Powered speaker
- Consumer Audio Equipment

Description

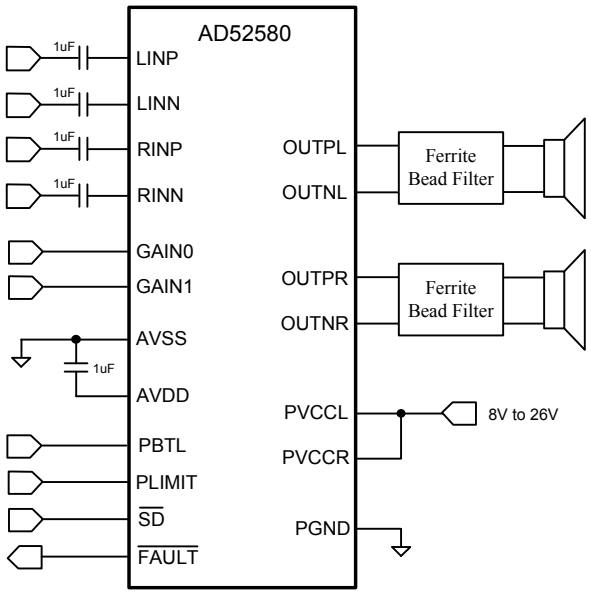
The AD52580 is a high efficiency stereo class-D audio amplifier with adjustable power limit function and dynamic temperature control. The loudspeaker driver operates from 8~26V supply voltage and analog circuit operates at 3.3V supply voltage. It can deliver 20W/CH output power into 8Ω loudspeaker within 0.09% THD+N and without external heat sink when playing music.

AD52580 provides parallel BTL (Mono) application, and it can deliver 40W into 4Ω loudspeaker within 0.15% THD+N. The adjustable power limit function allows user to set a voltage rail lower than half of 3.3V to limit the amount of current through the speaker.

Output DC detection prevents speaker damage from long-time current stress. The dynamic temperature control is a gain control system. As chip junction temperature higher than a warning level, the gain level will decrease until junction temperature lower than the warning level.

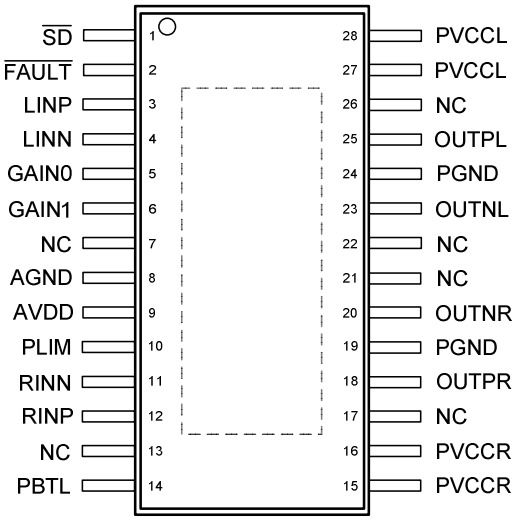
The output short circuit and over temperature protection include auto-recovery feature.

Simplified Application Circuit

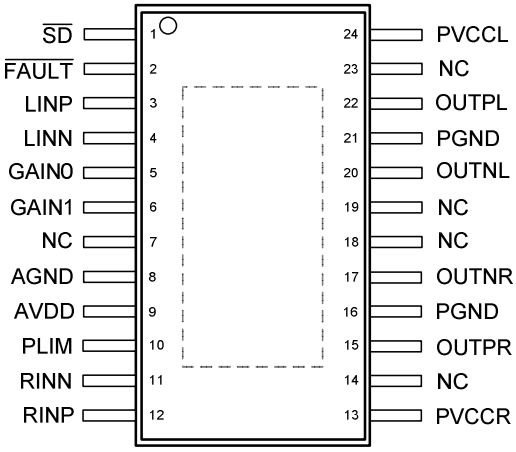


Pin Assignments

E-TSSOP-28L
(TOP VIEW)



E-TSSOP-24L
(TOP VIEW)



Pin Description

NAME	E-TSSOP -28L	E-TSSOP -24L	TYP	DESCRIPTION
$\overline{SD}$	1	1	I	Shutdown signal for IC (Low = disabled, output Hi-Z; High = operational). Voltage compliance to 26V.
$\overline{FAULT}$	2	2	O	Open drain output used to display short circuit or dc detect fault. Voltage compliant to 26V. Short circuit faults can be set to auto-recovery by connecting FAULTB pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVCC.
LINP	3	3	I	Positive audio input for left channel. Biased at 1.65V.
LINN	4	4	I	Negative audio input for left channel. Biased at 1.65V.
GAIN0	5	5	I	Gain select least significant bit. Voltage compliance to 26V.
GAIN1	6	6	I	Gain select most significant bit. Voltage compliance to 26V.
NC	7	7		Not connected.
AGND	8	8	P	Analog signal ground. Connect to the thermal pad.
AVDD	9	9	O	3.3V regulated output.
PLIMIT	10	10	I	Power limit level adjustment. Connect a resistor divider from AVDD to GND to set power limit. Give V(PLIMIT) < 1.55V to set power limit level. Connect to GND for no power limit.
RINN	11	11	I	Negative audio input for right channel. Biased at 1.65V.
RINP	12	12	I	Positive audio input for right channel. Biased at 1.65V.
NC	13	NA		Not connected.
PBTL	14	NA	I	Parallel BTL mode switch, high for parallel BTL output. Voltage compliance to 26V.

PVCCR	15,16	13	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
NC	17	14		Not connected.
OUTPR	18	15	O	Class-D H-bridge positive output for right channel.
PGND	19	16	P	Power ground for the H-bridges.
OUTNR	20	17	O	Class-D H-bridge negative output for right channel.
NC	21	18		Not connected.
NC	22	19		Not connected.
OUTNL	23	20	O	Class-D H-bridge negative output for left channel.
PGND	24	21	P	Power ground for the H-bridges.
OUTPL	25	22	O	Class-D H-bridge positive output for left channel.
NC	26	23		Not connected.
PVCCL	27,28	24	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
Thermal Pad			P	Must be soldered to PCB's ground plane.

Ordering Information

Product ID	Package	Packing	Comments
AD52580-QG24NAT	E-TSSOP 24L	62 Units / Tube 100 Tubes / Small Box	Green
AD52580-QG28NAT	E-TSSOP 28L	50 Units / Tube 100 Tubes / Small Box	Green
AD52580-QG28NAR	E-TSSOP 28L	2500 Units / Reel 5000 Units / Small Box	Green

Available Package

Package Type	Device No.	θ_{JA}(° C/W)	θ_{jc}(℃/W)	Ψ_{jt}(℃/W)	Exposed Thermal Pad
E-TSSOP 24L	AD52580	32.8	6.0	1.33	Yes (Note 1)
E-TSSOP 28L		28			

Note 1.1: ***The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is necessary.***

Note 1.2: ***θ_{ja} is measured on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.***

Note 1.3: ***θ_{jc} represents the heat resistance for the heat flow between the chip and the package's top surface.***

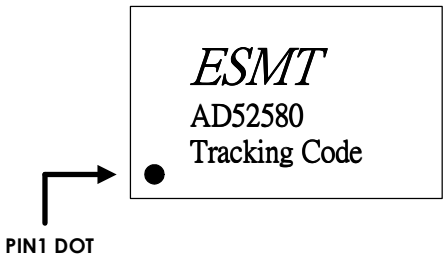
Note 1.4: Ψ_{jt} ***represents the heat resistance for the heat flow between the chip and the exposed pad's center.***

Marking Information

AD52580

- Marking Information

Line 1：LOGO
Line 2：Product No
Line 3：Tracking Code



Absolute Maximum Ratings

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
PVCC	Supply voltage	PVCCL, PVCCR	-0.3	30	V
V_I	Interface pin voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL, $\overline{FAULT}$,	-0.3	26	V
		PLIMIT	-0.3	3.6	
T_A	Operating free-air temperature range		-40	85	°C
T_J	Operating junction temperature range		-40	150	°C
T_{stg}	Storage temperature range		-65	150	°C
R_L	Minimum Load Resistance	BTL: PVCC ＞ 15V	4.8		Ω
		BTL: PVCC ≦ 15V	3.2		Ω
		PBTL	3.2		Ω

Recommended Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
PVCC	Supply voltage	PVCCL, PVCCR	8	26	V
V_{IH}	High-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL		0.8	V
V_{OL}	Low-level output voltage	$\overline{FAULT}$, $R_{PULL-UP}$=100k, PV_{CC}=26V		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, GAIN0, GAIN1, PBTL, V_I=2V, PV_{CC}=18V		50	uA
I_{IL}	Low-level input current	$\overline{SD}$, GAIN0, GAIN1, PBTL, V_I=0.8V, PV_{CC}=18V		5	uA
T_A	Operating free-air		-40	85	°C

General Electrical Characteristics

- PVCC=24V, R_L=8Ω, T_A=25°C (unless otherwise noted)

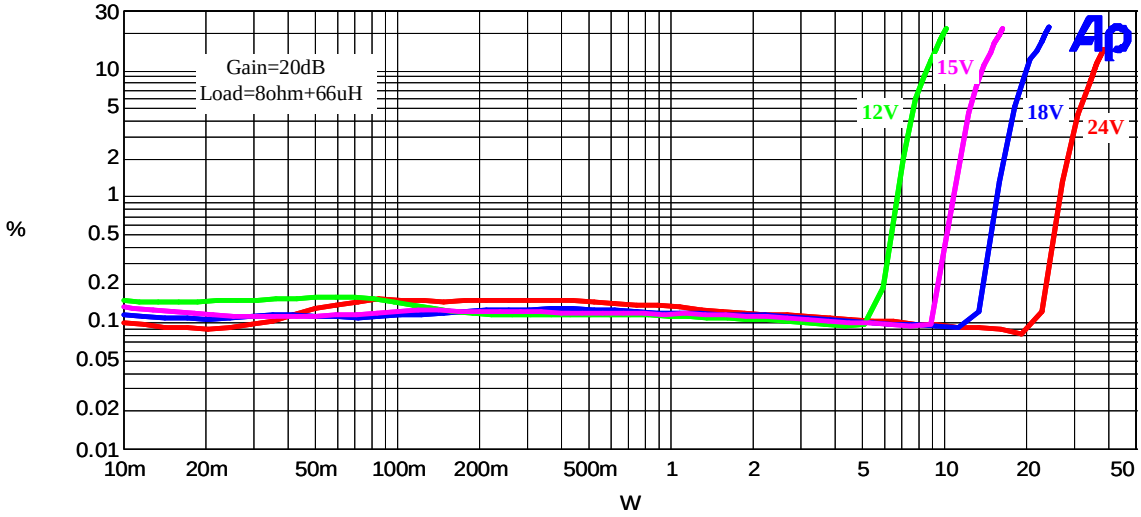
SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
$I_{CC(q)}$	Quiescent supply current	SD=2V, no load			32	50	mA
		SD=2V, no load, PVCC=12V			20	35	
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SD=0.8V, no load			< 10	25	uA
		SD=0.8V, no load, PVCC=12V			< 10	25	
$R_{DS(on)}$	Drain-source on-state resistance-High side PMOS	PVCC=12V, Id=500mA, T_J=25 °C			300		mΩ
	Drain-source on-state resistance-Low side NMOS				200		mΩ
$\|V_{OS}\|$	Class-D output offset voltage (measured differential)	V_I=0V, Gain=36dB				15	mV
t_{ON}	Turn-on time	SD=2V			12		ms
t_{OFF}	Turn-off time	SD=0.8V			4		μs
AVDD	Regulator output	I_{AVDD}=0.1mA		3.0	3.3	3.6	V
G	Gain	GAIN1 =0.8V	GAIN0=0.8V	18	20	22	dB
			GAIN0=2V	24	26	28	
		GAIN1 =2V	GAIN0=0.8V	30	32	34	
			GAIN0=2V	34	36	38	

Electrical Characteristics and Specifications of Loudspeaker Driver

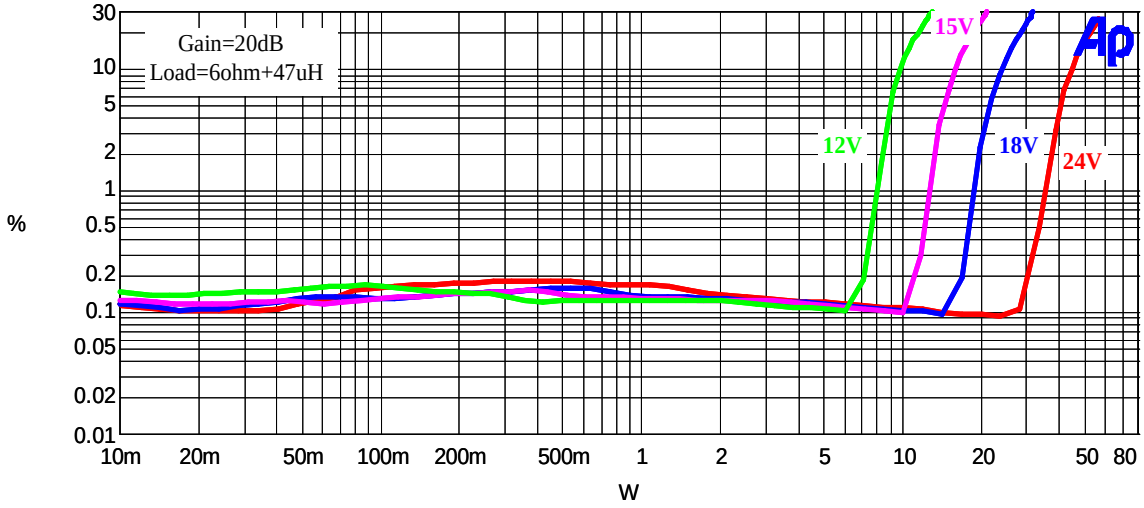
- PVCC=24V, R_L=8Ω, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P_O	Output power	THD+N=10%, f=1kHz, PVCC=16V		15		W
		THD+N=10%, f=1kHz, PVCC=13V		10		
THD+N	Total harmonic distortion plus noise	PVCC=16V, R_L=8Ω, f=1kHz, P_O=7.5W (half-power)		0.09		%
		PVCC=12V, R_L=8Ω, f=1kHz, P_O=5W (half-power)		0.11		
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f=1kHz, Gain=20dB, a-weighted		102		dB
V_n	Output integrated noise	F=20Hz ~ 20kHz, Gain=20dB, a-weighted filter, R_L=4Ω		145		μV
K_{SVR}	Power Supply Rejection Ratio	V_{ripple}=200mVpp at 1kHz, Gain=20dB, inputs ac-grounded		-62		dB
Crosstalk	Crosstalk	F=1kHz, V_O=1Vrms, Gain=20dB		-83		dB
f_{OSC}	Oscillator frequency		250	310		kHz
T_{SENSOR}	Thermal trip point			150		°C
	Thermal hysteresis			35		°C

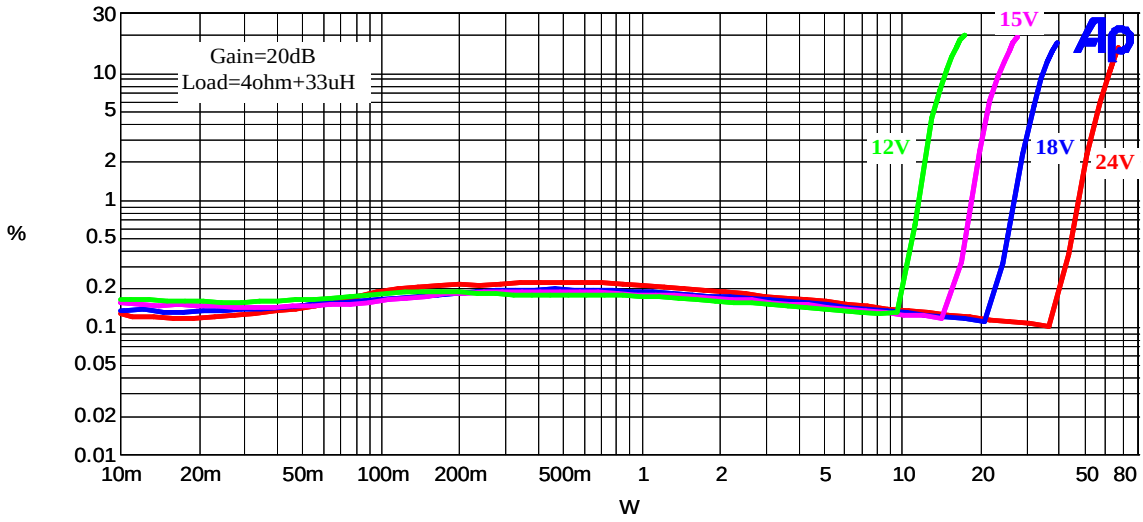
THD + N (%) v.s. Output power (8ohm load)



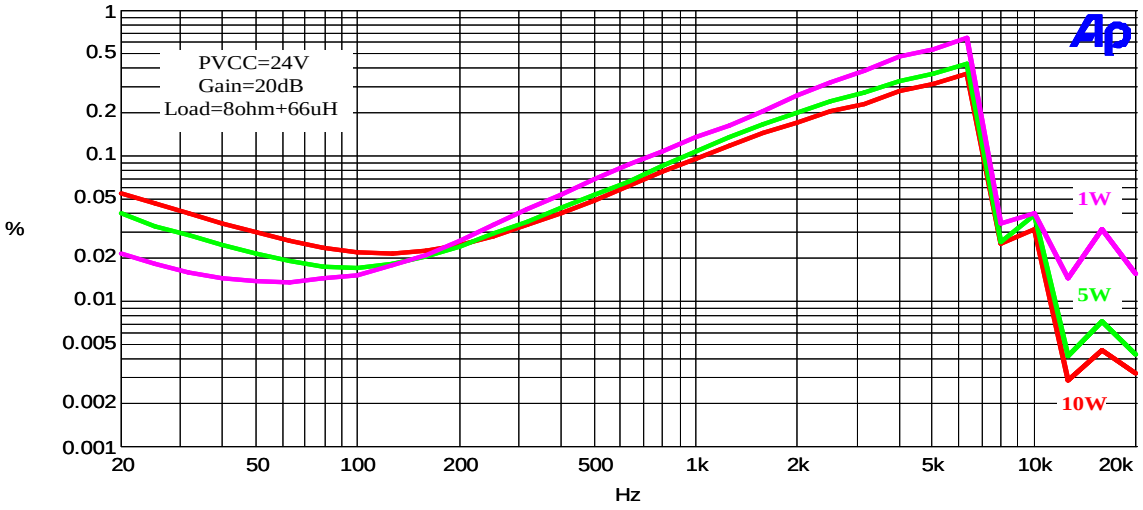
THD + N (%) v.s. Output power (6ohm load)



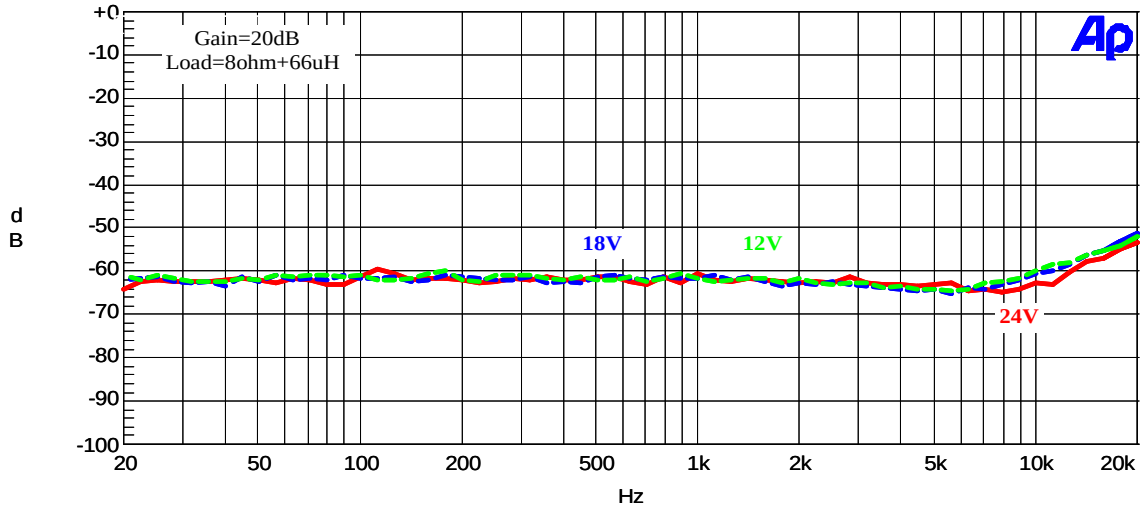
THD + N (%) v.s. Output power (4ohm load)



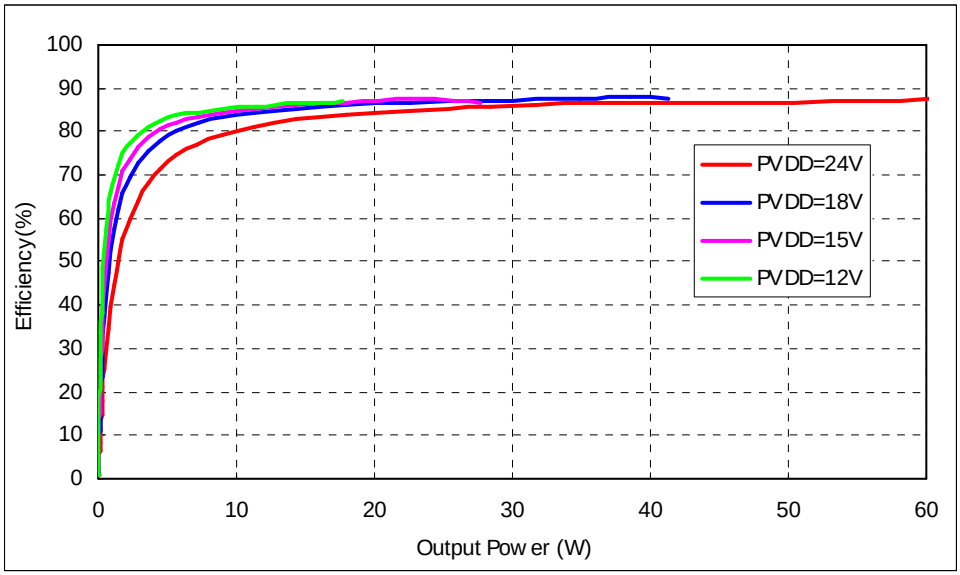
THD + N (%) v.s. Frequency (24V, 8ohm load)



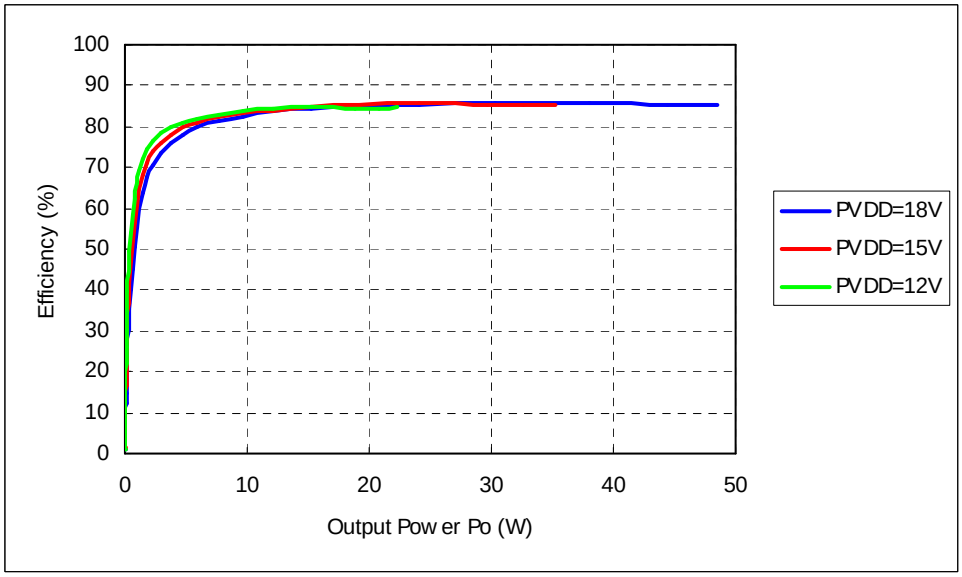
PSRR (24V, 8ohm load at Vripple=0.2Vpp)



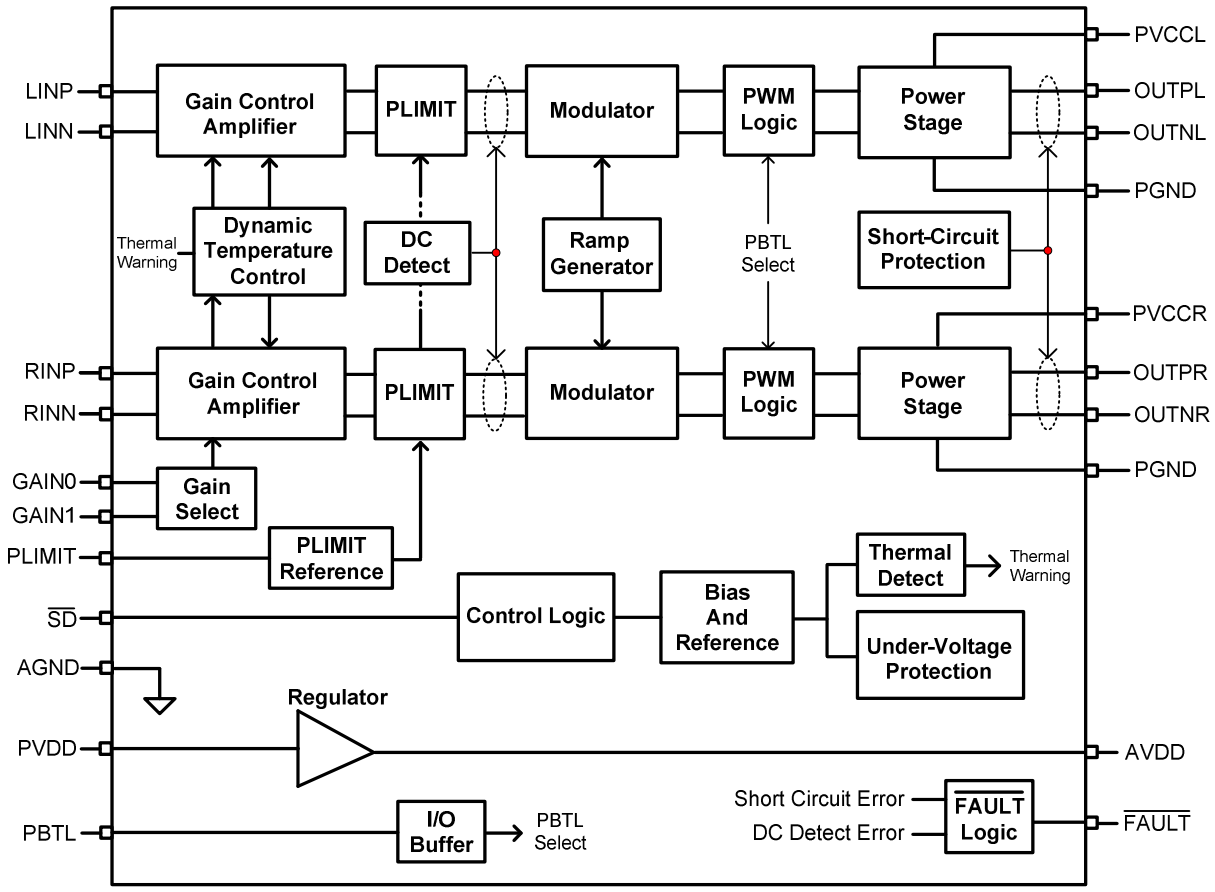
Efficiency (8ohm load) / 2ch



Efficiency (6ohm load) / 2ch



Functional Block Diagram



Operation Descriptions

- **Gain settings**

  The gain of the AD52580 is set by two input pins, GAIN0 and GAIN1. By varying input resistance in AD52580, the various volume gains are achieved. The respective volume gain and input resistance are listed in Table 1. However, there is 20% variation in input resistance from production variation.

Table 1. Volume gain and input impedance

GAIN1	GAIN0	Volume Gain (dB)	Input Resistance, R_{in} (kΩ)
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

- **Shutdown ($\overline{SD}$) control**

  Pulling $\overline{SD}$ pin low will let AD52580 operate in low-current state for power conservation. The AD52580 outputs will enter mute once $\overline{SD}$ pin is pulled low, and regulator will also disable to save power. If let $\overline{SD}$ pin floating, the chip will enter shutdown mode because of the internal pull low resistor. For the best power-off performance, place the chip in the shutdown mode in advance of removing the power supply.

- **DC detection**

  AD52580 has dc detection circuit to protect the speakers from DC current which might be occurred as input capacitor defect or inputs short on printed circuit board. The detection circuit detects first volume amplifier stage output, when both differential outputs' voltage become higher than a determined voltage or lower than a determined voltage for more than 420ms, the dc detect error will occur and report to $\overline{FAULT}$ pin. At the same time, loudspeaker drivers of right/left channel will disable and enter Hi-Z. This fault can not be cleared by cycling $\overline{SD}$, it is necessary to cycle the PVCC supply.

  The minimum differential input voltages required to trigger the DC detect function are shown in table2. The input voltage must keep above the voltage listed in the table for more than 420msec to trigger the DC detect fault. The equivalent class-D output duty of the DC detect threshold is listed in table3. For 24V supply, DC detect fault will occur as output duty exceed ±7% for more than 420msec.

Table 2. DC Detect Threshold (PVCC=24V)

AV (dB)	Vin (mV, differential)
20	317
26	159
32	80
36	50

Table 3. DC Detect Output Duty

PVCC (V)	Output Duty
8	±23%
12	±14.75%
16	±10.75%
24	±7%

- **Thermal protection**

  If the internal junction temperature is higher than 150°C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature for AD52580 returning to normal operation is about 115°C. The variation of protected temperature is about 10%. Thermal protection faults are NOT reported on the $\overline{\text{FAULT}}$ pin.

- **Short-circuit protection**

  To protect loudspeaker drivers from over-current damage, AD52580 has built-in short-circuit protection circuit. When the wires connected to loudspeakers are shorted to each other or shorted to VSS or to PVCC, overload detectors may activate. Once one of right and left channel overload detectors are active, the amplifier outputs will enter a Hi-Z state and the protection latch is engaged. The short protection fault is reported on $\overline{\text{FAULT}}$ pin as a low state. The latch can be cleared by reset $\overline{\text{SD}}$ or power supply cycling.

  The short circuit protection latch can have auto-recovery function by connect the $\overline{\text{FAULT}}$ pin directly to $\overline{\text{SD}}$ pin. The latch state will be released after 420msec, and the short protection latch will re-cycle if output overload is detected again.

- **Under-voltage detection**

  When the AVDD voltage is lower than 2.7V or the PVDD voltage is lower than 7.5V, loudspeaker drivers of right/left channel will be disabled and kept at low state. Otherwise, AD52580 return to normal operation.

- **Over-voltage protection**

  When the PVCC voltage is higher than 30V, loudspeaker will be disabled kept at low state. The protection status will be released as PVCC lower than 28.7V.

- **Power limit function**

  The voltage at PLIMIT pin (pin 10) can used to limit the power of first gain control amplifier output. Add a resistor divider from AVDD to ground to set the voltage V_{PLIMIT} at the PLIMIT pin. The voltage V_{PLIMIT} sets a limit on the output peak-to-peak voltage. The maximum BTL output voltage of the gain control amplifier is limited to $2*(1.55V–V_{PLIMIT})$. The Class-D BTL output voltage on loudspeaker is amplified by 9.95 of $2*(1.55V–V_{PLIMIT})$.

  For normal BTL operation (Stereo) and PBTL (Mono) operation:

$$P_{OUT} = \left[2 \times \left|V_P\right| \times 9.95\right]^2 \div \left(2 \times R_L\right) \quad \text{for unclipped power} \qquad (1)$$

  Where:

  - V_P is the peak voltage of gain control amplifier output,

    if $(V_{IN}*Gv\ /2) < (1.55V–V_{PLIMIT})$, then $V_P = (V_{IN}*Gv\ /2)$.
    If $(V_{IN}*Gv\ /2) > (1.55V–V_{PLIMIT})$, then $V_P = (1.55V–V_{PLIMIT})$.

  - V_{IN} is the input peak voltage.
  - Gv is the gain of gain control amplifier, the four gain levels are 1V/V, 2V/V, 4V/V, 6.34V/V, corresponding to 20dB, 26dB, 32dB, 36dB overall gain.
  - AVDD is the regulator output at pin 9, typical 3.3V.
  - R_L is the load resistance.

- P_{OUT} (10% THD) = 1.25 x P_{OUT} (unclipped).

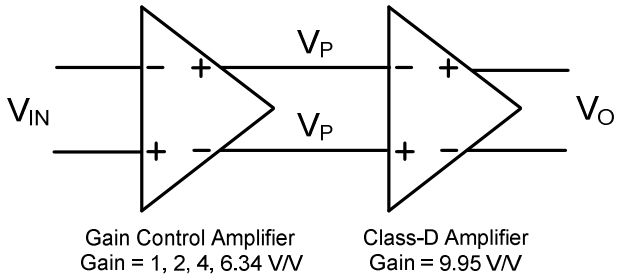


Figure 1. Gain Contribution of the Two Gain Stages

Table 4. PLIMIT Typical Operation

Test Conditions	Output P_O (W)	V_{PLIMIT} (V) @ THD+N=1%	V_{PLIMIT} (V) @ THD+N=10%	Output Voltage (Vp-p)
PVCC=24V RL=8Ω	25	0.54	0.65	40
	20	0.65	0.75	35.6
	15	0.77	0.85	30.8
	10	0.91	0.98	25.2
	5	1.1	1.15	17.8

Note: Connect PLIMIT pin to ground to disable power limit function.

- **PBTL (Mono) function (for product ID AD52580-QG28NAT only)**

  AD52580 provides the application of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin is tied high, the positive and negative outputs of left and right channel are synchronized and in phase. Apply the input signal to the RIGHT channel input in PBTL mode and let the LEFT channel input grounded, and place the speaker between the LEFT and RIGHT outputs. The output swing is doubled of that in normal mode. See the application circuit example for PBTL (Mono) mode operation. For normal BTL (Stereo) operation, connect the PBTL pin to ground.

- **Dynamic Temperature Control (DTC)**

  The DTC function is designed to protect the loudspeaker from over heating. As the junction temperature is higher than OT_W, the gain of amplifier will decrease step by step every 0.25s. Finally, as the junction temperature is lower than OT_R, the attenuated gain steps will be released step by step every 0.5s. If DTC can't suppress the temperature and the temperature reach to the OT trip point (150°C), the amplifier will be shutdown. The OT hysteresis temperature equals to OT_R. Typically, OT_W is 125°C and OT_R is 115°C.

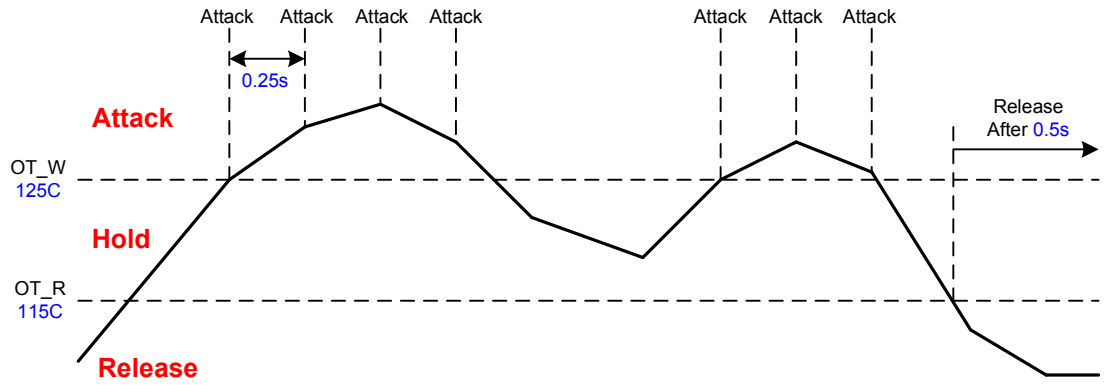


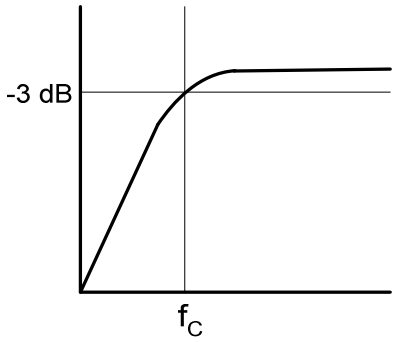
Figure 2. Dynamic Temperature Control Function

Application information

- **Input capacitors (C_{in})**

  The performance at low frequency (bass) is affected by the corner frequency (f_c) of the high-pass filter composed of input resistor (R_{in}) and input capacitor (C_{in}), determined in equation (2). Typically, a 0.1µF or 1µF ceramic capacitor is suggested for C_{in}. The resistance of input resistors is different at different gain setting. The respective gain and input resistance are listed in Table 1 (shown at GAIN SETTING). However, there is 20% variation in input resistance from production variation.

$$f_c = \frac{1}{2\pi R_{in} C_{in}} \ (\text{Hz}) \quad \cdots\cdots\cdots (2)$$



- **Ferrite Bead selection**

  If the traces from the AD52580 to speaker are short, the ferrite bead filters can reduce the high frequency emissions to meet FCC requirements. A ferrite bead that has very low impedance at low frequency and high impedance at high frequency (above 1MHz) is recommended. The impedance of the ferrite bead can be used along with a small capacitor with a value around 1000pF to reduce the frequency spectrum of the signal to an acceptable level.

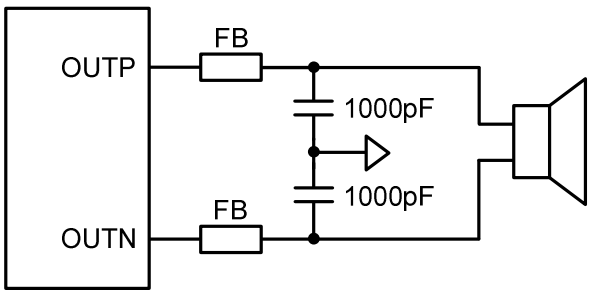


Figure 3. Typical Ferrite Bead Filter

- **Output LC Filter**

  If the traces from the AD52580 to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Figure 4 shows the typical output filter for 8Ω speaker with a cut-off frequency of 27 kHz and Figure 5 shows the typical output filter for 4Ω speaker with a cut-off frequency of 27 kHz.

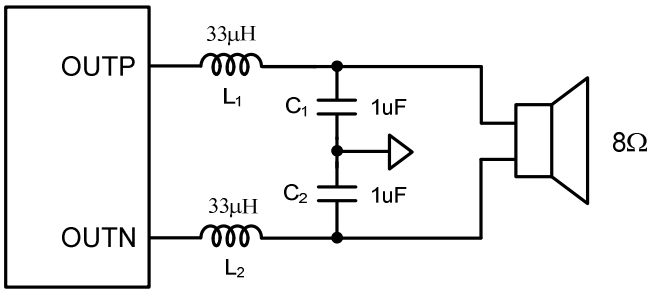


Figure 4. Typical LC Output Filter for 8Ω Speaker

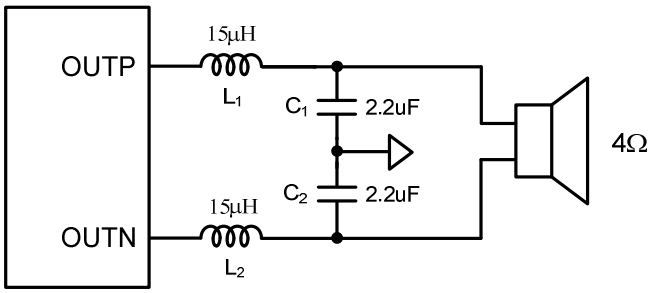


Figure 5. Typical LC Output Filter for 4Ω Speaker

- **Power supply decoupling capacitor (Cs)**

  Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVCC and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1µF or 1µF as close as possible to the device PVCC leads works best. For low frequency noise filtering, a 100µF or greater capacitor (tantalum or electrolytic type) is suggested.

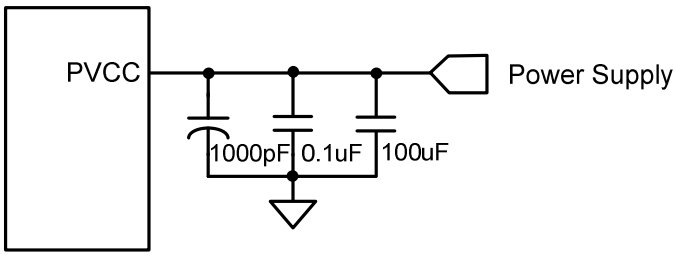
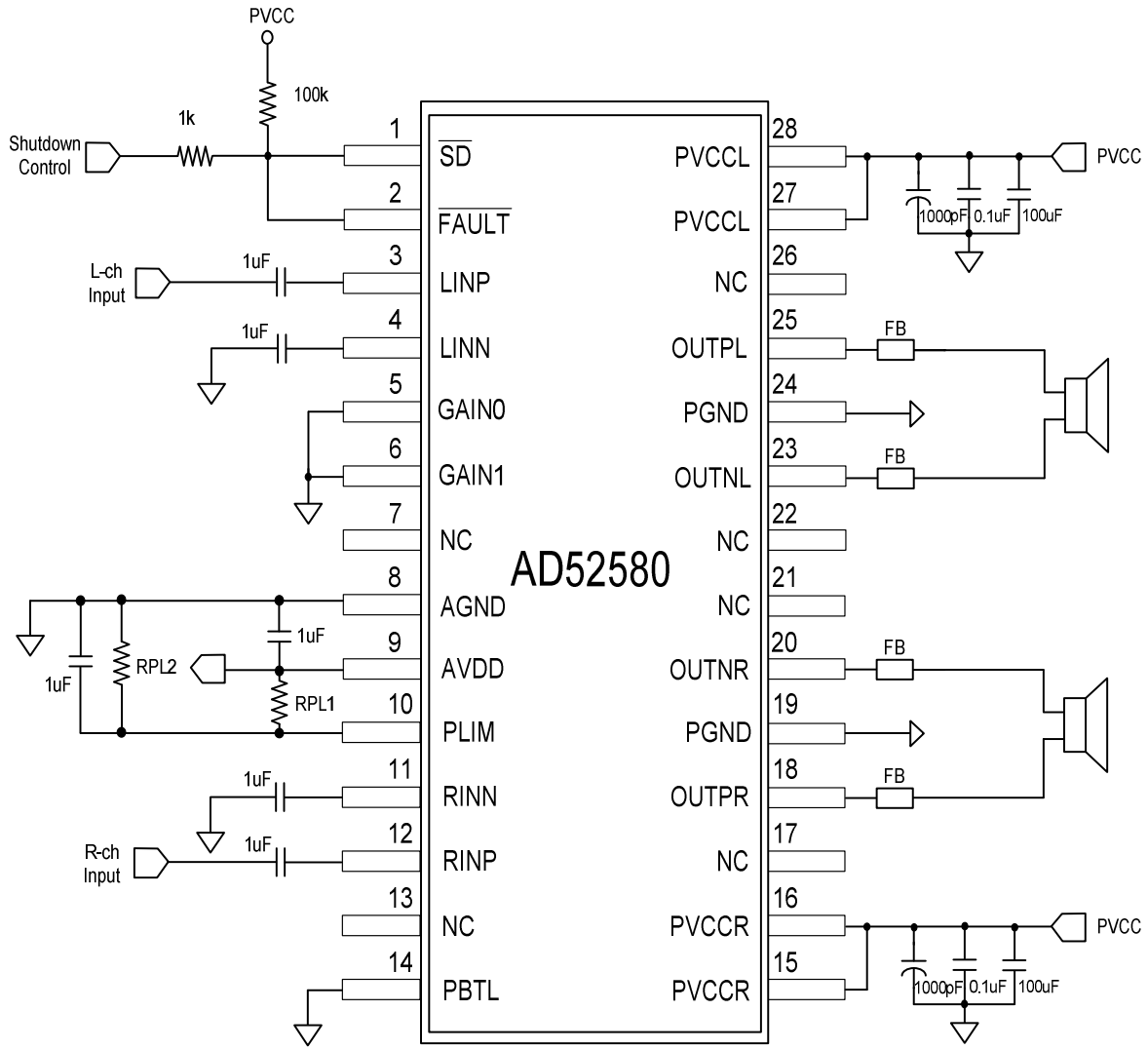


Figure 6. Recommended Power Supply Decoupling Capacitors.

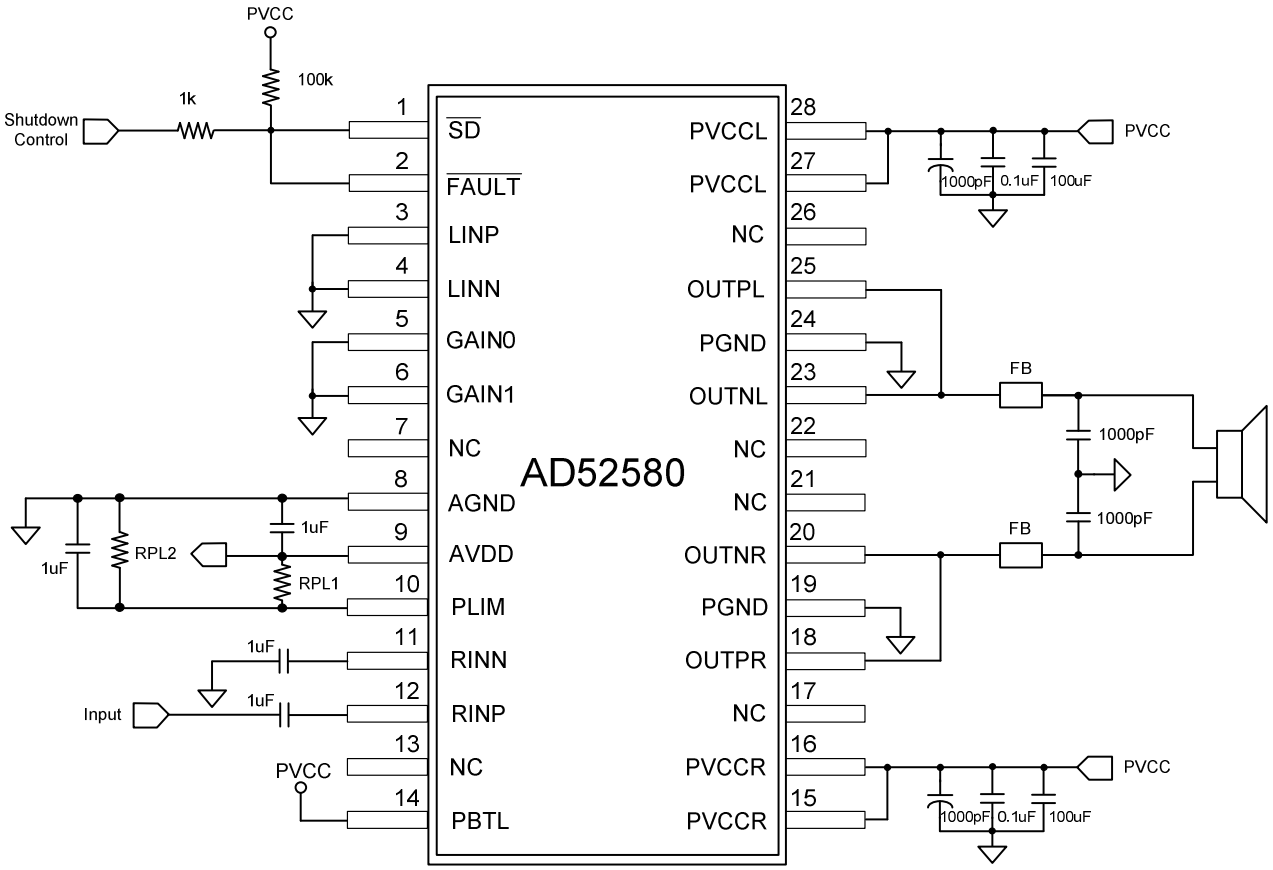
Application Circuit Example

- Application circuit for BTL (Stereo) mode configuration



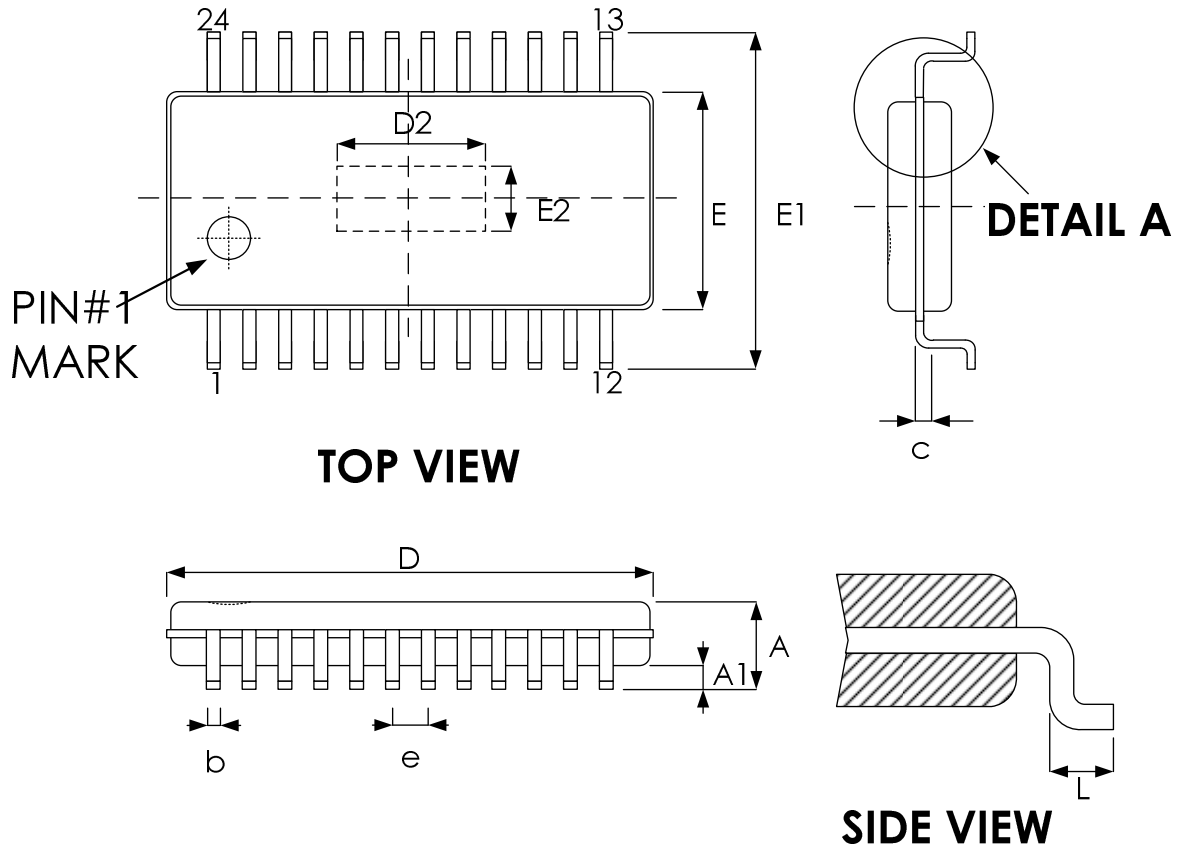
Application Circuit Example

- Application circuit for parallel BTL (Mono) mode configuration



Package Dimensions

- **E-TSSOP 24L**

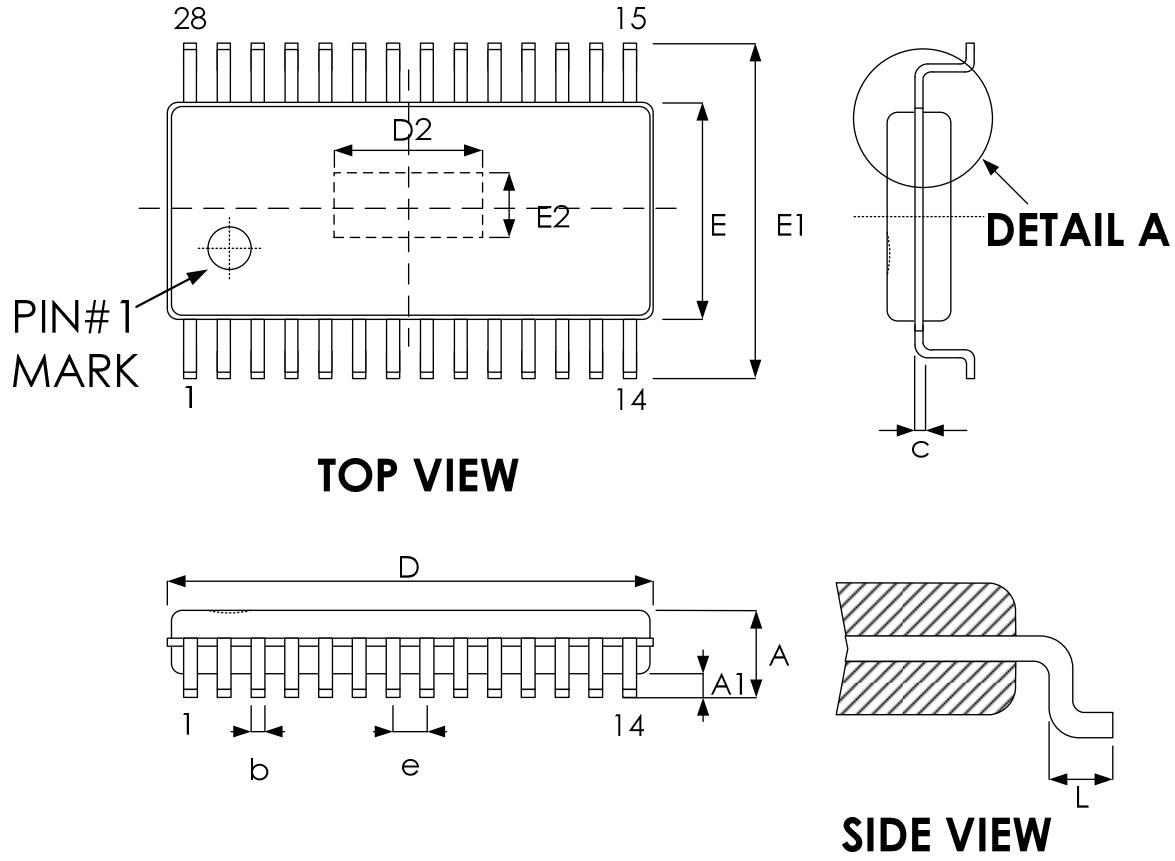


Symbol	Dimension in mm	
	Min	Max
A	1.00	1.20
A1	0.00	0.15
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
Option 1	Min	Max
D2	3.70	4.62
E2	1.50	1.88
Option 2		
D2	3.70	4.62
E2	2.20	2.85

- **E-TSSOP 28L**



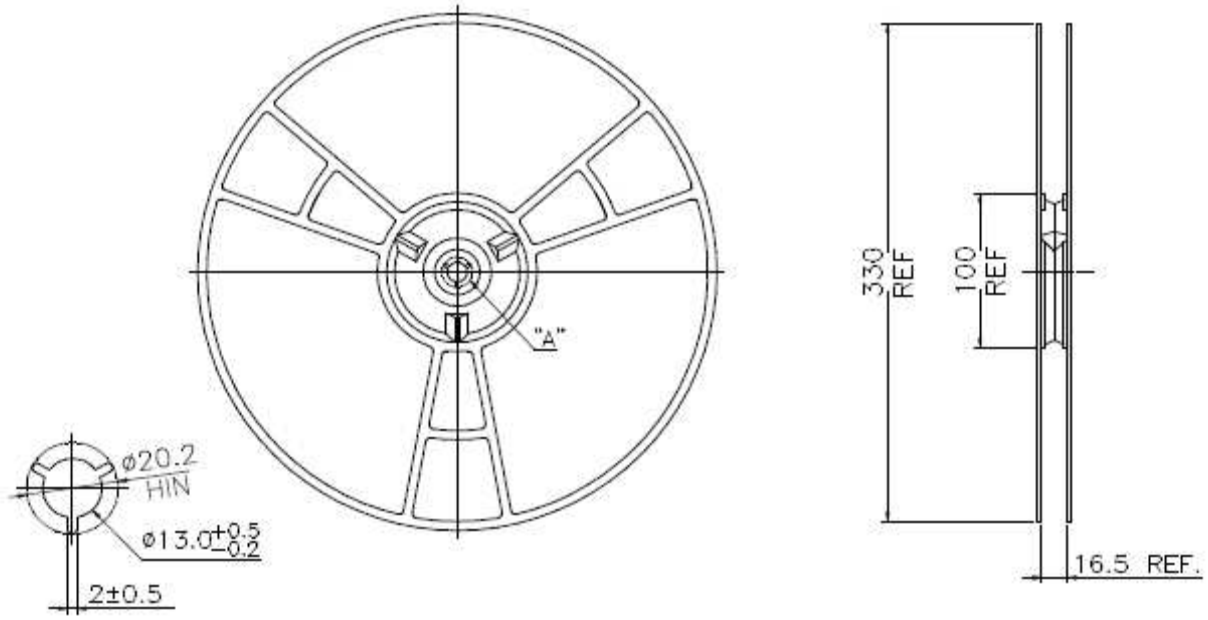
Symbol	Dimension in mm	
	Min	Max
A	0.00	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

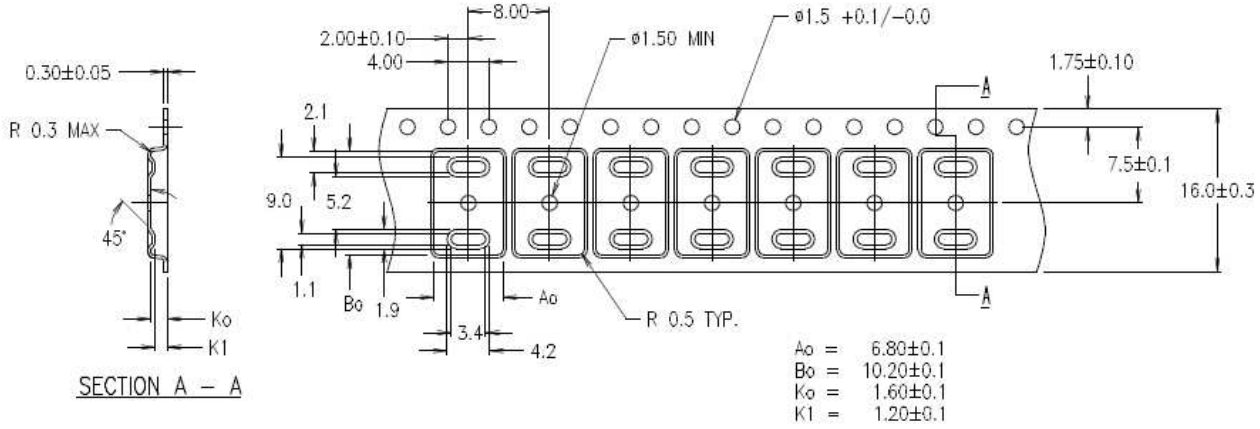
Exposed pad

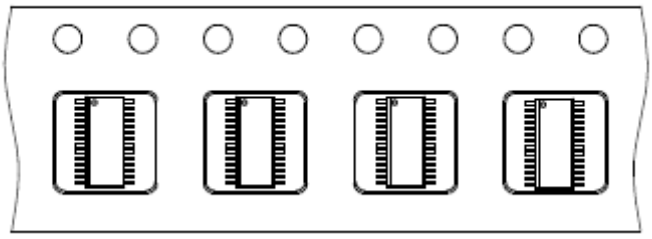
	Dimension in mm	
Option 1	Min	Max
D2	4.75	5.25
E2	2.56	2.97

TAPE AND REEL INFORMATION

Dimension in mm







Revision History

Revision	Date	Description
0.1	2012.07.18	Original.
1.0	2012.08	1. Skip “Preliminary” 2. Updated outline drawing 3. Modify power limit information 4. Added Mono application circuit
1.1	2013.01.30	1. Change Vn noise spec. 2. Change Package Dimensions 3. Change Frequency spec.
1.2	2013.08.27	1. add TSSOP-28 with T&R packing 2. add T&R dimension

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