SC8723 High Efficiency, Synchronous, 3.5A Buck-Boost Converter with Four Integrated MOSFETs

1 Descriptions

SC8723 is a synchronous 4-switch buck-boost converter with four integrated switches. It provides excellent power efficiency and voltage regulation no matter the output voltage is higher, lower or equal to the input voltage. SC8723 supports very wide input and output voltage range. It can support applications from 2.7V to 24V input range and 3V to 22V output range and provides up to 3.5A output current.

SC8723 employs average current-mode control. The output voltage is adjusted by FB pin with resistors. The switching mode (PSM /FPWM) and the switching frequency can be adjusted by external setting. The device also provides programmable output current limit which supports flexible design for different applications.

SC8723 supports internal current limit, input under voltage protection, output over voltage protection, output short protection, FB short circuit protection and over temperature protection to ensure safety under different abnormal conditions.

The IC is in a 22 pin 3x3 QFN package.

2 Features

- High Efficiency Buck-Boost Conversion
- Few External Components
- Integrated Low $R_{DS(ON)}$ Switches
- Wide VIN Range: 2.7 V to 24 V
- Wide VOUT Range:3V to 22V
- Fixed 5.1V VOUT with FB tied to GND
- Up to 3.5A Output Current
- 250K/500K/750K/1MHz Adjustable Switching Frequency
- Adjustable Output Current Limit
- Forced PWM Mode/ PSM Mode Selectable
- EN control and Programmable UVLO
- Internal Soft Start
- Absolute Input and Output Over Voltage Protection
- Output Short Protection with Hiccup Mode
- Thermal Shutdown Protection
- Under Voltage Protection
- Over Voltage Protection
- QFN-22 FC 3 x 3 Package

3 Applications

- USB Type C Hub
- Power Bank with Quick Charge
- Wireless Charger
- Wall Adapter
- Industry Power Supplies

4 Device Information

Part Number	Package	Dimension
SC8723QFKR	22 pin QFN	3.0mm x 3.0mm x 0.75mm

5 Typical Application Circuit

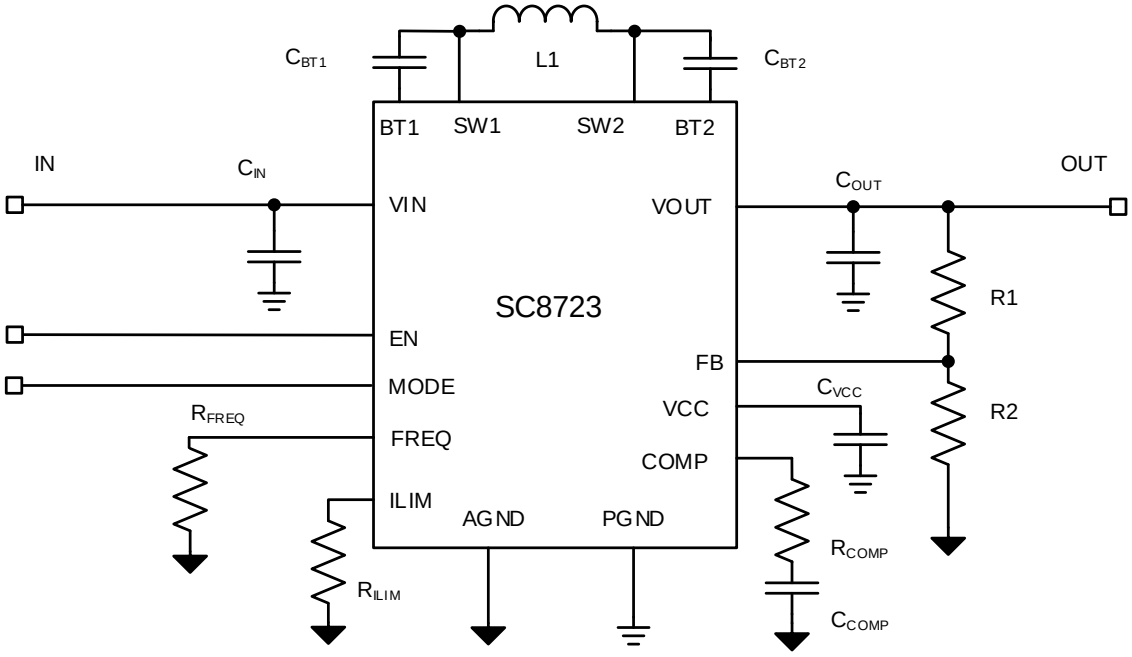
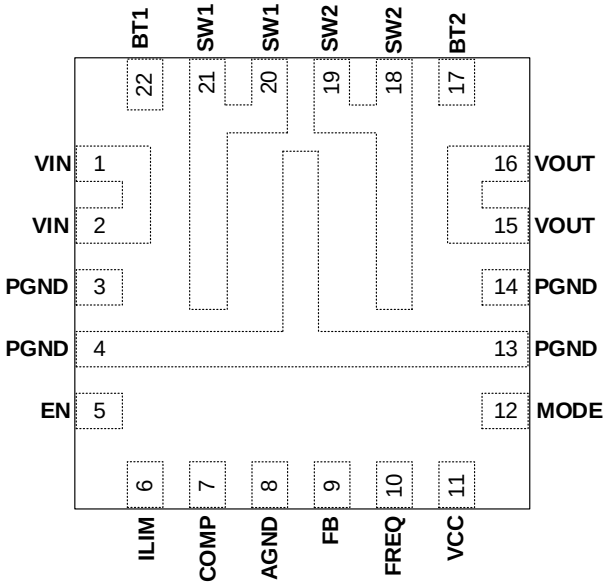


Figure1. Typical application circuit

6 Terminal Configuration and Functions

Top View



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1,2	VIN	PWR	The power input node of the converter.
3,4,13,14	PGND	PWR	Power ground. User shall connect PGND and AGND together on PCB.
5	EN	I	Enable logic input. Logic high level enables the device and logic low level disables the device.
6	ILIM	I	Connect a resistor to set the current limit value of output current.
7	COMP	I	Connect a RC network to compensate the control loop.
8	AGND	I/O	Analog ground. User shall connect PGND and AGND together on PCB.
9	FB	I	Feedback node of VOUT output voltage. Set the VOUT output voltage by the resistor divider connected at this pin. Output voltage be configured for fixed 5.1V with FB pin connected to GND.
10	FREQ	I	Set typical switching frequency of the device. FREQ pin ties to AGND: 250kHz (R_{FREQ} <20KΩ) FREQ pin keeps floating: 500kHz (R_{FREQ} >700KΩ) 50 KΩ < R_{FREQ} < 80KΩ: 750kHz 180 KΩ < R_{FREQ} < 320KΩ: 1MHZ The FREQ pin status is re-loaded when VIN power cycle or EN from low to high.

11	VCC	PWR	Output of an internal regulator. Connect a 1 μF ceramic capacitor from VCC to PGND pin close to the IC. The regulator provides supply for internal gate drivers.
12	MODE	I	Mode selection pin. Logic high level sets the device working in force PWM mode; logic low level or floating sets the device working in PSM mode. Connect to PGND to extend thermal performance if PSM mode is used.
15,16	VOUT	PWR	The power output node of the converter. Output voltage feedback node when FB short to ground is detected.
17	BT2	PWR	Connect a 100nF ceramic capacitor between BT2 pin and SW2 pin to provide the boosted bias voltage for high side gate driver.
18,19	SW2	PWR	Switching Node 2. Connect to inductor. Connect a 100nF ceramic capacitor between BT2 pin and SW2 pin to provide the boosted bias voltage for high side gate driver.
20，21	SW1	PWR	Switching Node 1. Connect to inductor. Connect a 100nF ceramic capacitor between BT1 pin and SW1 pin to provide the boosted bias voltage for high side gate driver.
22	BT1	PWR	Connect a 100nF ceramic capacitor between BT1 pin and SW1 pin to provide the boosted bias voltage for high side gate driver.

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	Unit
Voltage range at terminals(2)	MODE, ILIM, COMP, FB, FREQ, VCC	-0.3	6	V
	VIN, VOUT, SW1, SW2, EN	-0.3	28	V
	SW1, SW2 for less than 10ns	-4	28	V
	BT1 to SW1, BT2 to SW2	-0.3	6	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

6.2 Thermal Information(TBD)

THERMAL RESISTANCE(1)		QFN-22 (3mmX3mm)	UNIT
θ_{JA}	Junction to ambient thermal resistance	TBD	°C/W
θ_{JC}	Junction to case resistance	TBD	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

6.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	TBD	TBD	kV
	Charged device model (CDM) ESD stress voltage(3)	TBD	TBD	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

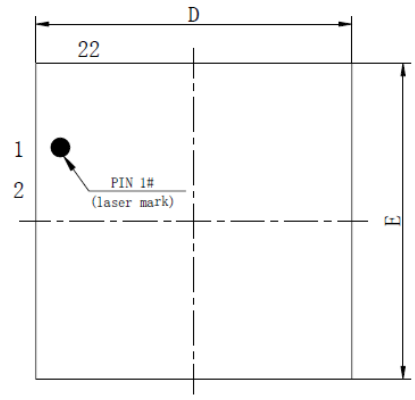
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

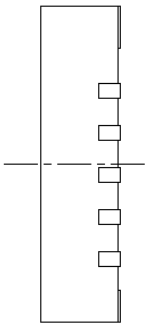
		MIN	MAX	UNIT
VIN	VIN voltage range	2.7	24	V
VOUT	VOUT voltage range	3	22	V

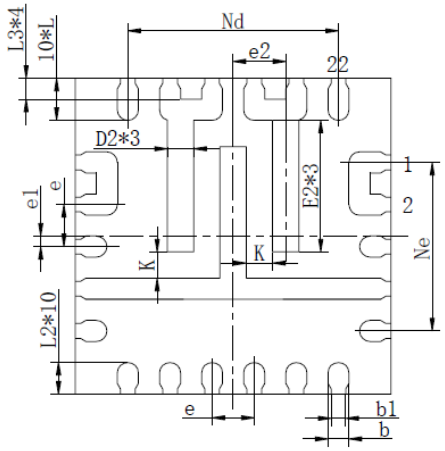
MECHANICAL DATA

QFN-22 (3x3x0.75)

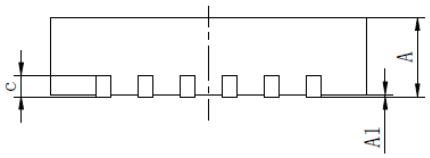


TOP VIEW





BOTTOW VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1		0.14REF	
c		0.203REF	
D	2.90	3.00	3.10
D2	0.15	0.25	0.35
Nd		2.00BSC	
e		0.40BSC	
e1		0.10BSC	
e2		0.50BSC	
E	2.90	3.00	3.10
E2	1.15	1.25	1.35
Ne		1.60BSC	
L	0.35	0.40	0.45
L2	0.25	0.30	0.35
L3	0.15	0.20	0.25
K		0.25REF	