

300mA Ultra Low I_Q Step-down DC/DC Converter With AOT Control

FEATURES

- Typ. 700nA Quiescent Current
- Adaptive On Time Control
- 2.5V to 5.5V Input Range
- Up to 93% Efficiency
- 16 Selectable Output Voltages in 100mV Steps between 1.8V to 3.3V
- Up to 300mA Output Current
- Automatic Transition to No Ripple 100% Mode
- Low Output Ripple Voltage
- Slew Rate Controlled Load Switch
- Discharge Function on VOUT / LOAD
- Power Good Output
- Optimized for Operation with a Tiny 2.2 μ H Inductor and 10 μ F C_{OUT}
- Small 2.4 x 2.4 mm² DFN-12 Package

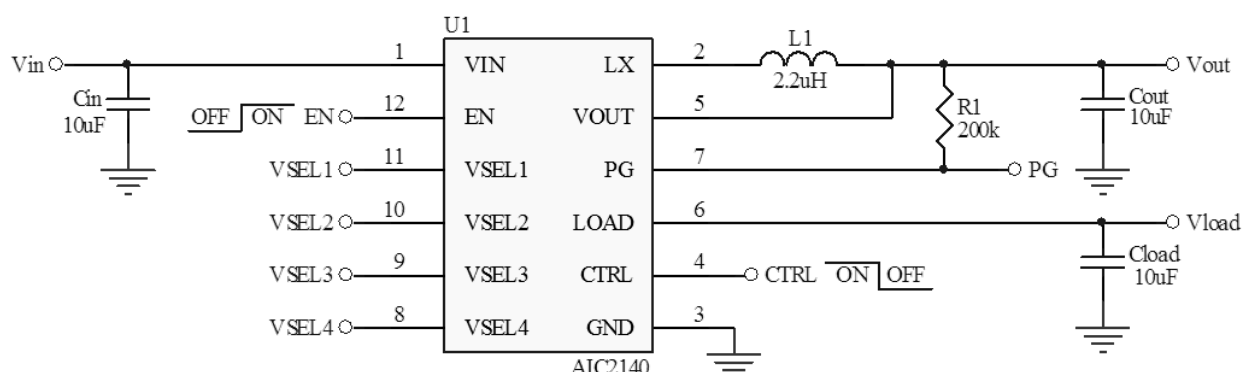
APPLICATIONS

- Wearable Device
- Bluetooth Low Energy
- Sensor HUB
- RF Module

DESCRIPTION

The AIC2140 is ultra low I_Q step-down dc/dc converter featuring typical 700nA quiescent current and operating with a tiny 2.2 μ H inductor and 10 μ F output capacitor. AIC2140 based device extends the light load efficiency range below 10 μ A load currents. AIC2140 supports output currents up to 600mA. The input voltage range from 2.5V to 5.5V allows also operation from a USB port and thin-film solar modules. The output voltage is user selectable by four VSEL pins within a range from 1.8V to 3.3V in 100mV steps. AIC2140 features low output ripple voltage and low noise with a small output capacitor. Once the battery voltage comes close to the output voltage (close to 100% duty cycle) the device enters no ripple 100% mode operation to prevent an increase of output ripple voltage. The device then stops switching and the output is connected to the input voltage. The integrated slew rate controlled load switch provides typical 0.6 Ω on-resistance and can distribute the selected output voltage to a temporarily used sub-system. The AIC2140 is available in a small 12 pin 2.4 x 2.4mm² DFN-12 package.

APPLICATIONS CIRCUIT



AIC2140 Application Circuit

ORDERING INFORMATION

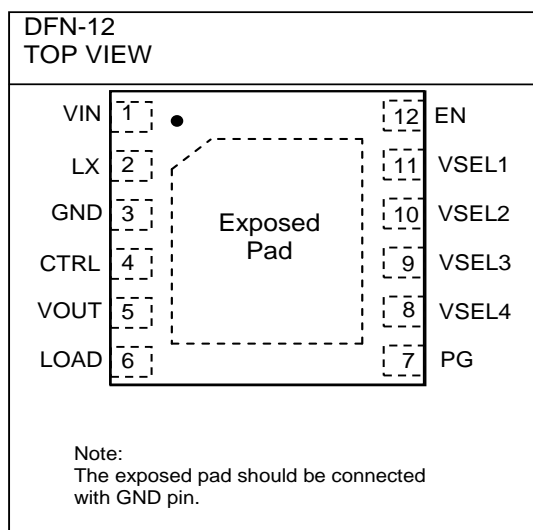
AIC2140 X XXX XX

PACKING TYPE
TR: TAPE & REEL
BG: BAG

PACKAGE TYPE
DBC: DFN-12
(2.4x2.4x0.45-0.4mm)

G: Green Package

PIN CONFIGURATION



Example: AIC2140GDBCTR

→ in DFN-12 Green Package and Tape
& Reel Packing Type

ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage, V_{IN}	6.0V
Pin Voltage for VOUT, LOAD	-0.3V to 3.7V
Pin Voltage for all other Pins	-0.3V to V_{IN}
Operating Ambient Temperature Range T_A	-40°C to 85°C
Operating Maximum Junction Temperature T_J	150°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Sec.)	260°C
Thermal Resistance Junction to Case DFN-12L (2.4x2.4 mm)*	10°C/W
Thermal Resistance Junction to Ambient DFN-12L (2.4x2.4 mm)*	65°C/W
(Assume no Ambient Airflow)	

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

*The package is placed on a two layers PCB with 2 ounces copper and 2 square inch, connected by 8 vias.

■ ELECTRICAL CHARACTERISTICS

($V_{IN}=3.6V$, unless otherwise specified. Typical values are at $T_A=25^{\circ}C$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
Operating Voltage	V_{IN}		2.5		5.5	V
Shutdown Current	I_{SHDN}	$V_{EN}=0V$, shutdown current into V_{IN}		70	1000	nA
Quiescent Current	I_Q	$V_{EN}=High$, CTRL=GND, $I_{OUT}=0mA$, $V_{OUT}=1.8V$, device not switching		700	1500	nA
Logic Threshold						
EN, CTRL, VSEL1-4 High Level Input Voltage	V_H	$2.5V \leq V_{IN} \leq 5.5V$			1.1	V
EN, CTRL, VSEL1-4 Low Level Input Voltage	V_L	$2.5V \leq V_{IN} \leq 5.5V$	0.4			V
Output Discharge Switch (VOUT)						
MOSFET on-resistance	R_{DSCH_VOUT}	$V_{IN} = 3.6V$, EN = GND, $I_{OUT} = -10mA$ into VOUT pin		10	30	Ω
Bias current into VOUT pin	I_{IN_VOUT}	$V_{IN} = 3.6V$, EN = High, $V_{OUT} = 2V$, CTRL =GND		130	200	nA
Load Output (LOAD)						
R_{LOAD}	High Side MOSFET on-resistance	$I_{LOAD} = 50mA$, CTRL = High, $V_{OUT} = 2.0V$, $2.5V \leq V_{IN} \leq 5.5V$		0.8	1.25	Ω
R_{RDSCH_LOAD}	Low Side MOSFET on-resistance	CTRL = GND, $2.5V \leq V_{IN} \leq 5.5V$, $I_{LOAD} = -10mA$		10	30	Ω
t_{Rise_LOAD}	V_{LOAD} rise time	Starting with CTRL low to high transition, time to ramp V_{LOAD} from 0V to 95% $V_{OUT} = 1.8V$, $2.5V \leq V_{IN} \leq 5.5V$, $I_{LOAD} = 1mA$		200	800	μs
Auto 100% Mode Transition						
Auto 100% Mode leave detection threshold	V_{TH_100+}	Rising V_{IN} , 100% Mode is left with $V_{IN} = V_{OUT} + V_{TH_100+}$, max value at $T_J = 85^{\circ}C$		250		mV
Auto 100% Mode enter detection threshold	V_{TH_100-}	Falling V_{IN} , 100% Mode is entered with $V_{IN} = V_{OUT} + V_{TH_100-}$, max value at $T_J = 85^{\circ}C$		250		mV
Switch On Resistance						
High Side Switch On Resistance	$R_{DS(ON)H}$	$V_{IN} = 3.6V$, $I_{out} = 50mA$		0.55	0.85	Ω
Low Side Switch On Resistance	$R_{DS(ON)L}$	$V_{IN} = 3.6V$, $I_{out} = 50mA$		0.22	0.5	Ω

■ ELECTRICAL CHARACTERISTICS (Continuous)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output						
Output Voltage Range	V_{OUT}	Output voltages are selected with pins VSEL 1 - 4	1.8		3.3	V
Output Voltage Accuracy		$V_{IN} = 3.6V, V_{OUT}=1.8V$	-2		2	%
Line Regulation		$V_{OUT} = 1.8V, CTRL = V_{IN}, I_{OUT} = 10\text{ mA}, 2.5V \leq V_{IN} \leq 5.5V$		0.1		%/V
Load Regulation		$V_{OUT} = 1.8V, V_{IN} = 3.6V, CTRL = V_{IN}$		0.005		%/mA
Regulator start up delay time	$t_{Startup_delay}$	$V_{IN} = 3.6V$, from transition EN = low to high until device starts switching		2.5	5	ms
Softstart time with reduced switch current limit	$t_{Softstart}$	$2.5V \leq V_{IN} \leq 5.5V, EN = V_{IN}$		800	1200	μs
High side MOSFET switch current limit	$I_{LIM_softstart}$	Reduced switch current limit during softstart	80	150		mA
Current Limit						
High Side Switch Forward Current Limit	I_{LIMIT}	$V_{IN}=3.6V$	480	600		mA
On-Time Timer Control						
Minimum On-Time	t_{ON}	$V_{IN}=3.6V, V_{OUT}=1.8V$		333		ns
Minimum Off-Time	$t_{OFF(MIN)}$	$V_{IN}=2.5V$		60		ns
Power Good						
PGOOD Threshold	V_{TH_PG}	Rising output voltage on VOUT pin, referred to V_{VOUT}		97.5		%
	V_{PG_Hys}	Hysteresis		2		
PGOOD Output Low	V_{OL_PG}	$2.5V \leq V_{IN} \leq 5.5V, EN=GND$, current into PG pin $I_{PG} = 4mA$			0.3	V
Bias Current Into PG Pin	I_{IN_PG}	PG pin is high impedance, $V_{OUT}=2V, EN=V_{IN}, CTRL = GND, I_{OUT}=0mA$		0	10	nA
Under Voltage Lockout Voltage						
UVLO Threshold	V_{UVLO+}	Raising Input Voltage		2.15	2.45	V
	V_{UVLO-}	Falling Input Voltage		1.95	2.4	V

Note 1: Specifications are production tested at $T_A=25^{\circ}C$. Specifications over the $-40^{\circ}C$ to $85^{\circ}C$ operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

TYPICAL PERFORMANCE CHARACTERISTICS

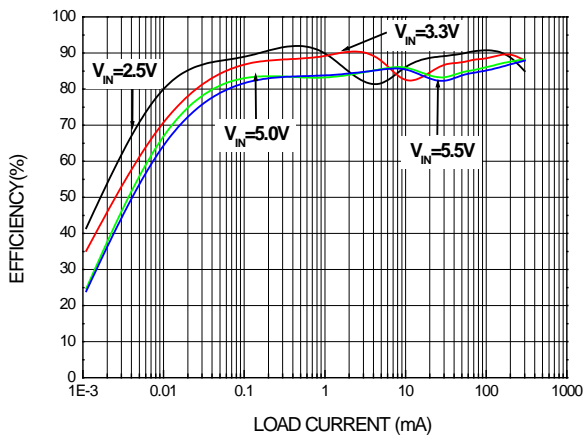


Fig. 1 Efficiency vs. Output Current ($V_{OUT}=1.8V$)

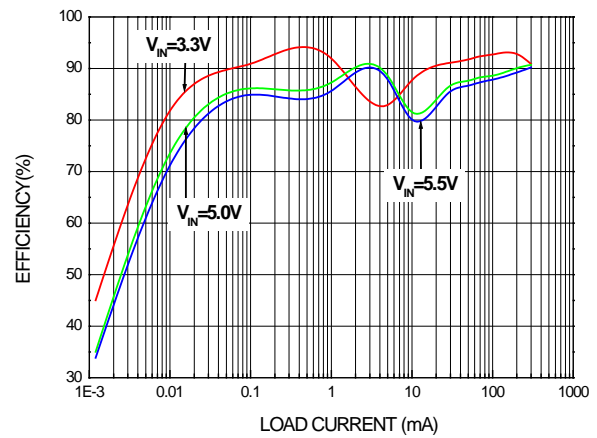


Fig. 2 Efficiency vs. Output Current ($V_{OUT}=2.5V$)

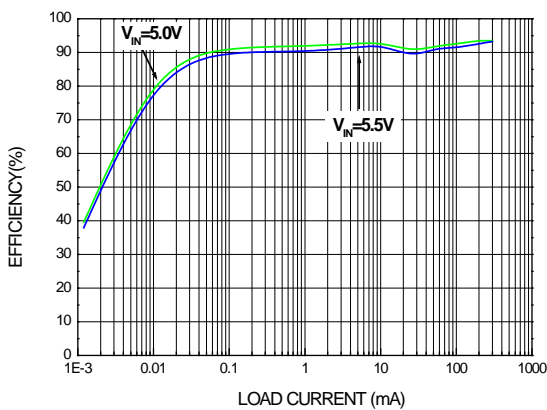


Fig. 3 Efficiency vs. Output Current ($V_{OUT}=3.3V$)

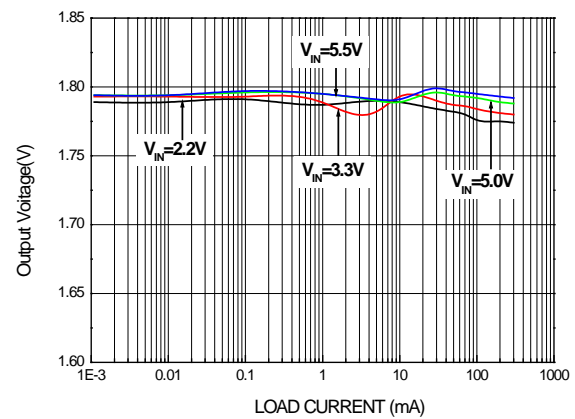


Fig. 4 Output Voltage vs. Output Current ($V_{OUT}=1.8V$)

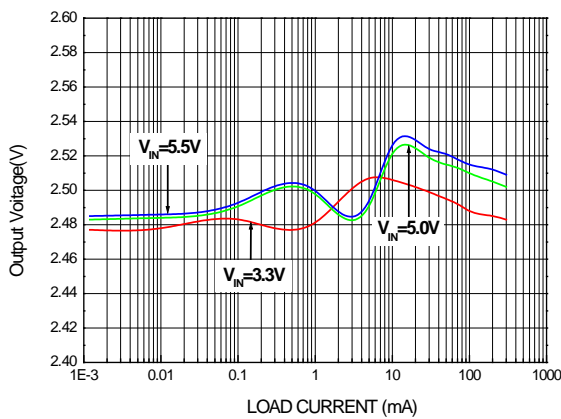


Fig. 5 Output Voltage vs. Output Current ($V_{OUT}=2.5V$)

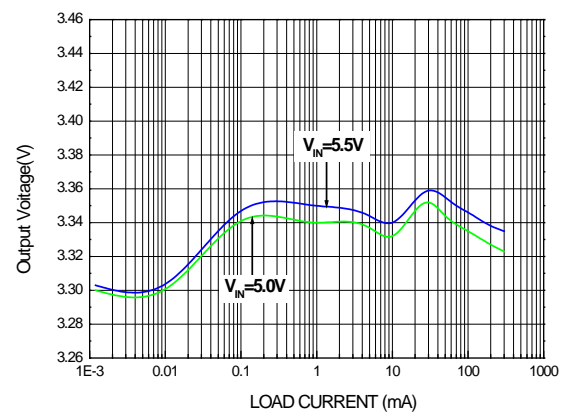


Fig. 6 Output Voltage vs. Output Current ($V_{OUT}=3.3V$)

TYPICAL PERFORMANCE CHARACTERISTICS (Continuous)

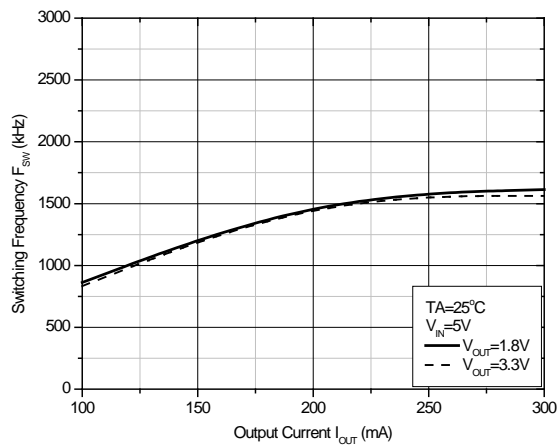


Fig. 7 Frequency vs. Output Current

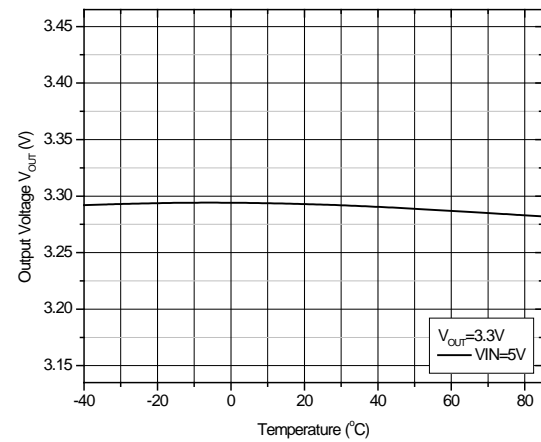


Fig. 8 Output Voltage vs. Temperature

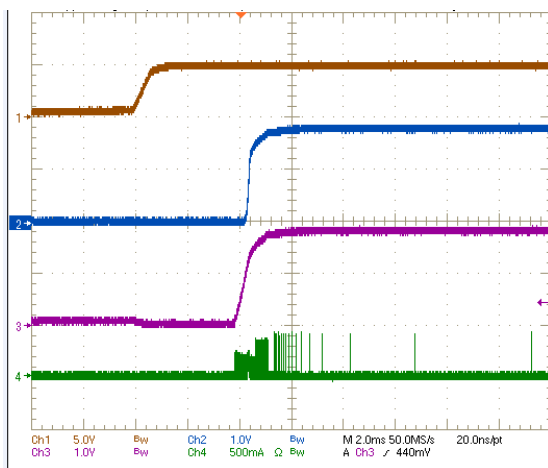

(CH1: V_{IN} , CH2: V_{PG} , CH3: V_{OUT} , CH4: I_L)

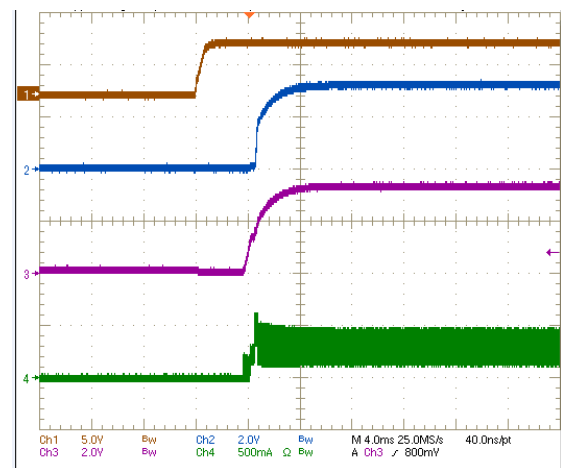
Fig. 9 V_{IN} Power On ($V_{IN} = 5\text{V}$, $V_{OUT} = 3.3\text{V}$, $I_{OUT} = 0\text{A}$)

(CH1: V_{IN} , CH2: V_{PG} , CH3: V_{OUT} , CH4: I_L)

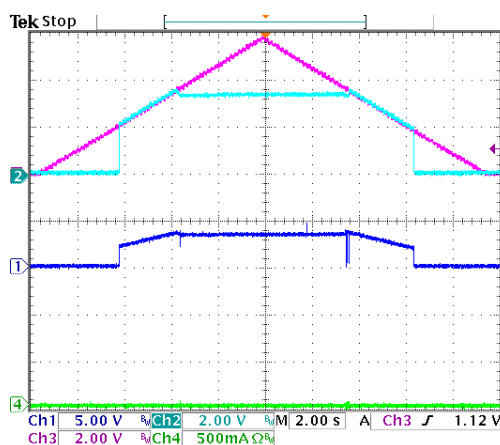
Fig. 10 V_{IN} Power On ($V_{IN} = 5\text{V}$, $V_{OUT} = 3.3\text{V}$, $I_{OUT} = 0.3\text{A}$)

(CH1: V_{IN} , CH2: V_{OUT} , CH3: V_{LX} , CH4: I_L)

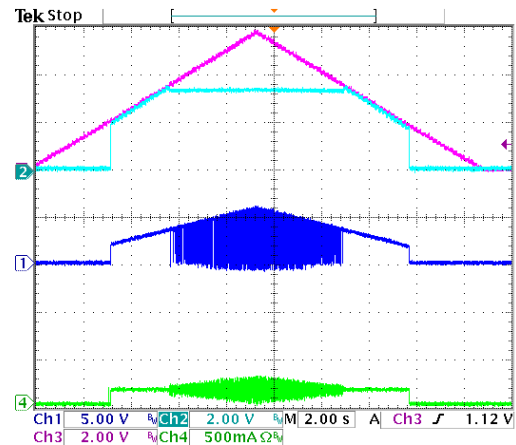
Fig. 11 100% Duty Cycle ($V_{IN} = 0 \sim 5\text{V}$, $V_{OUT} = 3.3\text{V}$, $I_{OUT} = 0\text{A}$)

(CH1: V_{IN} , CH2: V_{OUT} , CH3: V_{LX} , CH4: I_L)

Fig. 12 100% Duty Cycle ($V_{IN} = 0 \sim 5\text{V}$, $V_{OUT} = 3.3\text{V}$, $I_{OUT} = 0.15\text{A}$)

■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

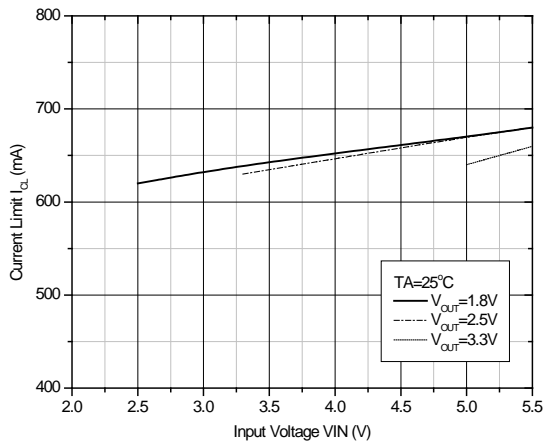


Fig. 13 Current Limit vs. Input Voltage

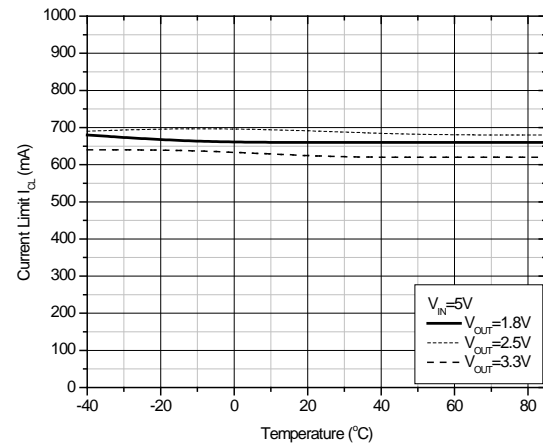


Fig. 14 Current Limit vs. Temperature

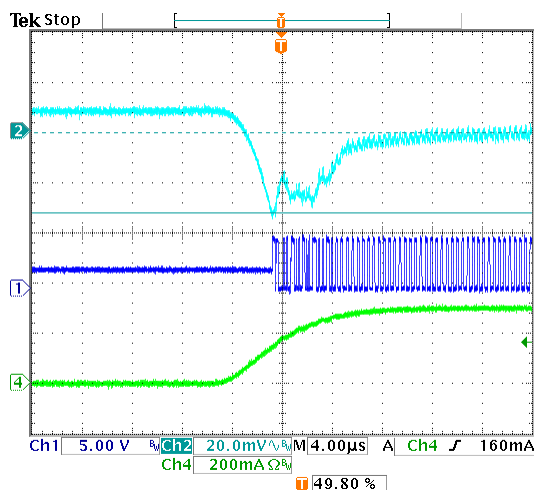


Fig. 15 Load Transient ($V_{IN} = 5\text{V}$, $V_{OUT} = 1.8\text{V}$, $I_O = 0-0.3\text{A}$)

The schematic diagram illustrates the internal architecture of the LT8602 buck converter in 100% duty mode. Key components and their connections include:

- Inputs:** VIN (1.2V), EN (enable), CTRL (load switch control), LOAD, VOUT (0.6V), and four sense inputs (VSEL1, VSEL2, VSEL3, VSEL4).
- Control Loop:** A feedback loop consisting of a Reference Generator, a Slope Generator, a Comparator (COMP), and an On-Time Control block. The Reference Generator provides VREF to the Comparator and the On-Time Control block. The Slope Generator provides a sawtooth signal to the Comparator. The Comparator's output drives the On-Time Control block, which generates the DON (done) signal.
- Driver and Output:** The On-Time Control block drives the Driver, which provides PGATE and NGATE signals to the power MOSFETs. The Driver also provides a ZCD (Zero Current Detect) signal.
- 100% Duty Mode:** A 100% Duty Mode block receives VINQR and VOUTQR signals and provides a feedback signal to the Comparator.
- Other Components:** An OTP (One-Time Programmable) memory, a ZCD (Zero Current Detect) comparator, and a ZCD (Zero Current Detect) output are also shown.

Functional Block Diagram of AIC2140

Pin Number	Pin Name	Pin Function
1	VIN	Power Input Supply. Decouple this pin to GND with a capacitor.
2	LX	Internal Power MOSFET Switches Output. Connect this pin to the inductor.
3	GND	Ground. Connect this pin to the negative terminal of C _{IN} , C _{OUT} and C _{LOAD} .
4	CTRL	The LOAD output control pin. The LOAD output is disabled when CTRL is low. This pin isn't allowed to float.
5	VOUT	Output Voltage Sense Pin. An internal power switch is connected between this pin and the LOAD pin. Connect this pin directly to the output capacitor with a short trace.
6	LOAD	The LOAD output. An internal power switch connects the LOAD pin to the VOUT pin when CTRL is high. The LOAD output is connected to GND by an internal discharge switch when CTRL is low. If not used, leave the pin open.
7	PG	Power Good Indicator.
8	VSEL4	Output voltage selection pin.
9	VSEL3	Output voltage selection pin.
10	VSEL2	Output voltage selection pin.
11	VSEL1	Output voltage selection pin.
12	EN	Enable Pin. Connect to logic high in normal operation. Forcing this ping to GND causes the device to be shutdown. This pin isn't allowed to float.

■ APPLICATION INFORMATION

The AIC2140 is an adaptive on-time control synchronous step down converter that can maintain almost fixed switching frequency over full input voltage range. It can deliver up to 600mA output current from 2.5V to 5.5V input voltage. Unlike the traditional fixed frequency PWM control, the adaptive on-time control has the simpler control circuit and the faster transient response. During normal operation, the AIC2140 can regulate its output voltage through a feedback control circuit, which is composed of a comparator, a slope generator, a reference generator and several control signal generators. At the beginning of the switching cycle, the main power switch will be turned on and the synchronous power switch will be turned off. The main power switch will be turned off after the internal on-time timer expires. When the main power switch is turned off, the synchronous power switch will be turned on until the summing signal of feedback voltage signal and slope signal is lower than reference voltage signal or the inductor current starts to reverse. The AIC2140 will enter discontinuous conduction mode (DCM) operation while working at light load conditions.

CTRL

When CTRL pin is set logic high, an internal power switch will connect the VOUT pin to the LOAD pin to power up an additional sub-system. By connecting the CTRL to GND, the LOAD pin will be disconnected from the VOUT pin and connected to GND by an internal discharge switch. At this operation mode, the voltage of LOAD pin will reduce to 0V.

Enable

When EN pin is set logic high, AIC2140 is put into active mode operation. By connecting the EN pin to GND, the device can be shutdown to reduce the supply to 0.07 μ A (typical). At this operation mode, the VOUT pin is connected to GND by an internal

discharge switch and the output voltage of step-down converter will reduce to 0V.

Soft Start

AIC2140 provides the soft-start function to prevent a large inrush current and output overshoot during start up period. During the soft-start period, the soft-start signal will limit the feedback threshold voltage at FB pin. When the soft-start signal voltage is higher than reference voltage, the feedback threshold voltage at FB pin reaches the desired value. The soft-start time is about 800 μ s (typical).

Power Good Indicator

AIC2140 contains an on-chip comparator for power good detection. If the output voltage is lower than power good low threshold, the output voltage of PG pin will be pulled low.

Over Current Protection

The AIC2140 provides cycle-by-cycle current limit function by using an internal over current protection circuit. When the main power switch turns on, the inductor current follows through the main power switch and the internal over current protection circuit senses it. While the peak value of inductor current gets higher than current limit threshold, the current limitation function is activated. While the current limitation function is activated, cycle-by-cycle current limit protection directly limits inductor peak current to protect the internal power switches.

100% Duty Cycle Operation

When the input voltage falls below the 100% duty cycle mode enter threshold, the AIC2140 will stop switching and enter 100% duty cycle operation mode. In 100% duty cycle mode, the output voltage is equal to the input voltage minus the voltage, which is the drop across the main power switch and the inductor.

The AIC2140 will exit from the 100% duty cycle operation mode and start switching again once the input voltage gets higher than the 100% duty cycle mode leave threshold.

Components Selection

Inductor

A 2.2μH inductor is recommended for most AIC2140 applications. Although small size and high efficiency are major concerns, the inductor should have low core losses at operation frequency and low ESR. For most designs, the inductance value can be derived from the following equations:

$$L \geq \frac{V_{OUT}}{f_{OSC} \cdot \Delta I_L} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Where ΔI_L is the inductor ripple current.

In addition, it is important to ensure the inductor saturation current exceeds the peak value of inductor current in application to prevent core saturation. The peak inductor current can be calculated from:

$$I_{PEAK} = I_{OUT(max)} + \frac{V_{OUT}}{2 \times f_{OSC} \cdot L} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Input Capacitor Selection

To prevent the high input voltage ripple and noise resulted from high frequency switching, the use of low ESR ceramic capacitor for the maximum RMS current is recommended. The approximated RMS current of the input capacitor can be calculated according to the following equation.

$$I_{CINRMS} \approx \sqrt{I_{OUT(MAX)}^2 \times \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}^2} + \frac{\Delta I_L^2}{12}}$$

Low ESR, X5R or X7R, ceramic capacitors are ideal for this function. The capacitor should be placed as close to the IC as possible for the best. At least a

10μF ceramic capacitor is suggested for the input capacitor.

Output Capacitor Selection

The selection of output capacitor depends on the required output voltage ripple. The output voltage ripple can be expressed as:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times f_{OSC} \cdot C_{OUT}} + ESR \cdot \Delta I_L$$

The output capacitor limits the output ripple during large load transient. For low output voltage ripple, the use of low ESR, X5R or X7R, ceramic capacitor is recommended. When choosing output capacitors, the voltage rating of output capacitor should be higher than the output voltage. 10μF ceramic capacitor may be needed for the output capacitor.

Setting the Output Voltage

The AIC2140 doesn't require an external resistor divider to set the output voltage. The output voltage can be programmed by the output voltage selection pins. AIC2140 supports an output voltage range of 1.8V to 3.3V in 0.1V steps. The output voltage can be set according to Table 1.

Table 1 Output Voltage Setting

V _{OUT} (V)	VSEL4	VSEL3	VSEL2	VSEL1
1.8	Low	Low	Low	Low
1.9	Low	Low	Low	High
2.0	Low	Low	High	Low
2.1	Low	Low	High	High
2.2	Low	High	Low	Low
2.3	Low	High	Low	High
2.4	Low	High	High	Low
2.5	Low	High	High	High
2.6	High	Low	Low	Low
2.7	High	Low	Low	High
2.8	High	Low	High	Low
2.9	High	Low	High	High
3.0	High	High	Low	Low
3.1	High	High	Low	High
3.2	High	High	High	Low
3.3	High	High	High	High

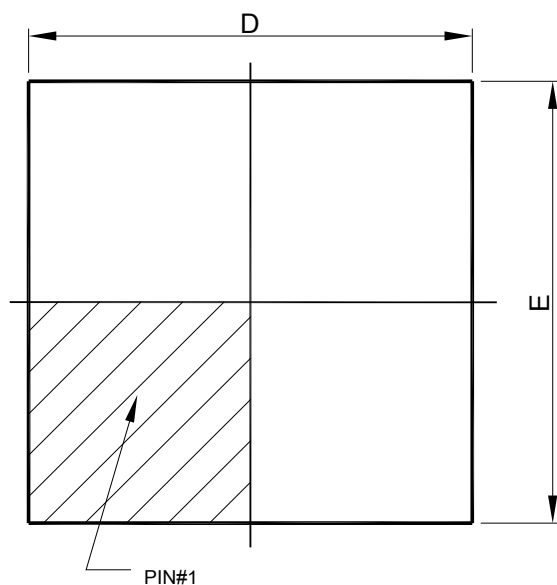
PCB Layout Guidance

In order to ensure a proper operation of AIC2140, the following points should be managed comprehensively.

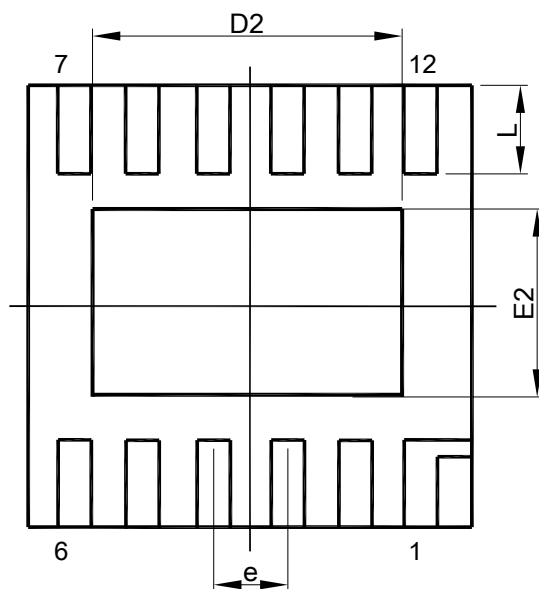
1. The input capacitor and V_{IN} should be placed as close as possible to each other to reduce the input voltage ripple and noise.
2. The output loop, which is consisted of the inductor, the internal power switches and the output capacitor, should be kept as small as possible.
3. The routes with large current should be kept short and wide.
4. Logically the large current on the converter should flow at the same direction.
5. In order to prevent the effect from noise, the IC's GND pin should be placed close to the ground of the input bypass capacitor.
6. The VOUT pin should be connected to the output capacitor directly with a short trace and the route should be away from the noise sources.

PHYSICAL DIMENSIONS (unit: mm)

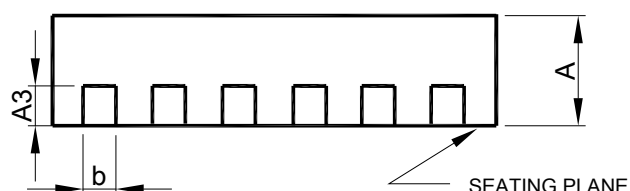
DFN-12 (2.4x2.4x0.45-0.4)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Note : 1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER , CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.

SYMBOL	DFN-12 (2.4x2.4x0.45-0.4)	
	MILLIMETERS	
	MIN.	MAX.
A	0.40	0.50
A3	0.127 BSC	
b	0.13	0.25
D	2.35	2.45
D2	2.10	2.30
E	2.35	2.45
E2	1.20	1.40
e	0.40 BSC	
L	0.30	0.40

Note:

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