LM5166 3-V to 65-V Input, 500-mA Synchronous Buck Converter with Ultra-Low I_Q

1 Features

- Wide 3-V to 65-V Input Voltage Range
- 9.7-µA No-Load Quiescent Current
- -40°C to 150°C Junction Temperature Range
- Meets EN55022 and CISPR 22 EMI Standards
- Integrated 1-Ω PFET Buck Switch
  - Supports 100% Duty Cycle for Low Dropout
- Integrated 0.5-Ω NFET Synchronous Rectifier
  - Eliminates External Schottky Diode
- Programmable Peak Current Limit Supports:
  - 500 mA, 300 mA, or 200 mA Loads
- Fixed (5 V, 3.3 V) or Adjustable V_{OUT} Options
- Two Selectable Control Options:
  - COT for Nearly Constant Frequency
  - PFM for Maximum Efficiency
- 1.223-V ±1.2% Internal Voltage Reference
- Switching Frequency up to 600 kHz
- 900-µs Internal or Externally Adjustable Soft-Start
- Diode Emulation and Pulse Skipping for Ultra-High Light-Load Efficiency
- No Loop Compensation or Bootstrap Components
- Precision Enable/Input UVLO with Hysteresis
- Open-Drain Power Good Indicator
- Thermal Shutdown Protection with Hysteresis
- Pin-to-pin Compatible with the LM5165
- 10-Pin, 3-mm x 3-mm VSON Package

2 Applications

- Industrial control systems
- High voltage LDO replacement
- Low power bias supplies
- Automotive and battery-powered applications

3 Description

The LM5166 is a compact, easy-to-use, 3-V to 65-V, ultra-low I_Q synchronous buck converter with high efficiency over wide input voltage and load current ranges. With integrated high-side and low-side power MOSFETs, up to 500 mA of output current can be delivered at fixed output voltages of 3.3 V or 5 V, or an adjustable output. The converter is designed to simplify implementation while providing options to optimize the performance for the target application. Pulse Frequency Modulation (PFM) mode is selected for optimal light-load efficiency or Constant On-Time (COT) control for nearly constant operating frequency. Both control schemes do not require loop compensation while providing excellent line and load transient response and short PWM on-time for large step-down conversion ratios.

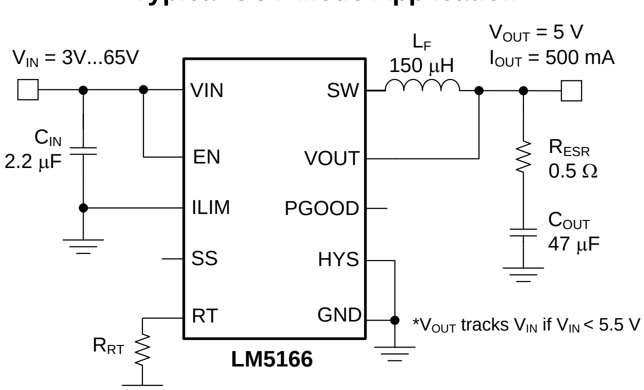
The high-side p-channel MOSFET can operate at 100% duty cycle for lowest dropout voltage and does not require a bootstrap capacitor for gate drive. Also, the current limit setpoint is adjustable to optimize inductor selection for a particular output current requirement. Selectable/adjustable startup timing options include minimum delay (no soft-start), internally fixed (900 µs), and externally programmable soft-start via an external capacitor. An open-drain PGOOD indicator can be used for sequencing and output voltage monitoring. The LM5166 is available in a VSON-10 package with 0.5-mm pin pitch. To create a custom regulator design, use the LM5166 with WEBENCH® *Power Designer.*

Device Information(1)

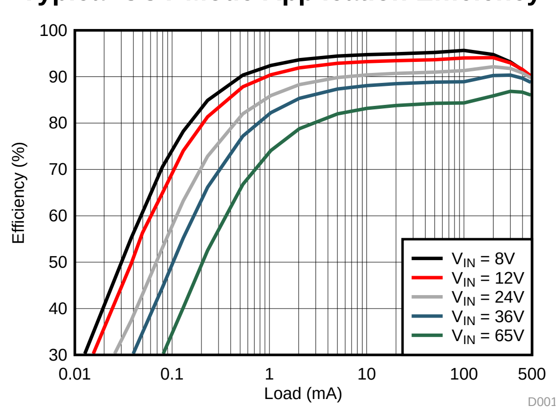
ORDER NUMBER	PACKAGE	BODY SIZE (NOM)
LM5166	VSON (10)	3 mm x 3 mm
LM5166X		
LM5166Y		

(1) For all available package, see the Package Option Addendum at the end of the datasheet.

Typical COT Mode Application



Typical COT Mode Application Efficiency



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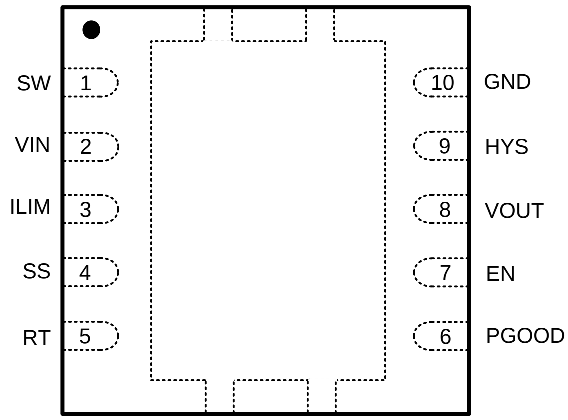
4 Revision History

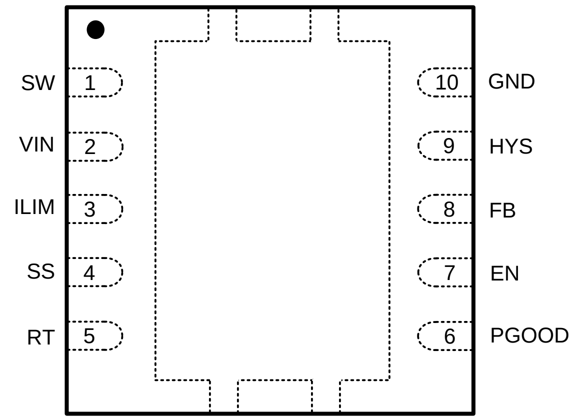
DATE	REVISION	NOTES
December 2016	*	Initial release.

5 Pin Configuration and Functions

VSON
10-Pin
Top View



LM5166X, LM5166Y
Fixed Output Versions



LM5166
Adjustable Output Version

Pin Functions

PIN		I/O (1)	DESCRIPTION
NUMBER	NAME		
1	SW	P	Switching node that is internally connected to the drain of the PFET buck switch (high side) and the drain of the NFET synchronous rectifier (low side). Connect to the filter inductor.
2	VIN	P	Regulator supply input pin to high-side power MOSFET and internal bias rail LDO. Connect to input supply and input filter capacitor C_{IN}. The path from the VIN pin to the input capacitor must be as short as possible.
3	ILIM	I	Programming pin for current limit. Connecting the appropriate resistance from the ILIM pin to GND selects one of the three current limit options. The available current limit options are detailed in Table 3.
4	SS	I	Programming pin for the soft-start delay. If a 100-kΩ resistor is connected from the SS pin to GND, the internal soft-start circuit is disabled and the FB comparator reference steps immediately from zero to full value when the regulator is enabled by the EN input. If the SS pin is left open, the internal soft-start circuit ramps the FB reference from zero to full value in 900 µs. If a capacitor is connected from the SS pin to GND, the soft-start time can be set longer than 900 µs.
5	RT	I	Mode select and on-time programming pin for Constant On-Time control. Connect a resistor from the RT pin to GND to program the on-time and hence switching frequency. Short RT to GND to select PFM (pulse frequency modulation) operation.
6	PGOOD	O	Power Good output flag pin. PGOOD is connected to the drain of an NFET that holds the pin low when either FB or VOUT is not in regulation. Use a 10-kΩ to 100-kΩ pullup resistor to system voltage rail or VOUT (no higher than 12 V).
7	EN	I	Input pin of the precision enable / UVLO comparator. The regulator is enabled when the EN pin voltage is greater than 1.22 V.
8	VOUT or FB	I	Feedback input to the voltage regulation loop. VOUT pin connects the internal feedback resistor divider to the regulator output voltage for the fixed 3.3-V or 5-V options. FB pin connects the internal feedback comparator to an external resistor divider for the adjustable voltage option. The reference for the FB pin comparator is 1.223 V.
9	HYS	O	Drain of internal NFET that is turned off when the EN input is greater than the EN pin threshold. External resistors from HYS to EN and GND program the input UVLO threshold and hysteresis.
10	GND	G	Regulator ground return.
-	PAD	P	Connect to GND pin and system ground on PCB. Path to C_{IN} must be as short as possible.

(1) P = Power, G = Ground, I = Input, O = Output.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
VIN		–0.3	68	V
EN		–0.3	(V_{VIN} + 0.3)	V
SW		–0.7	(V_{VIN} + 0.3)	V
	20-ns transient	–3		
PGOOD, VOUT(3)		–0.3	16	V
HYS		–0.3	7	V
ILIM, SS, RT, FB(4)		–0.3	3.6	V
T_J	Maximum junction temperature(5)	–40	150	°C
T_L	Lead temperature(6)		200	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Fixed output setting.
(4) Adjustable output setting.
(5) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.
(6) For detailed information on soldering plastic SO PowerPAD packages, refer to SNOA549 available from Texas Instruments. Maximum solder time not to exceed 4 seconds.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input voltages	VIN	3		65	V
	EN	–0.3		V_{VIN}	
	PGOOD	–0.3		12	
	HYS	–0.3		5.5	
Output current	I_{OUT}	0		500	mA
Temperature	Operating junction temperature (2)	–40		150	°C

(1) Operating Ratings are conditions under which the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC[1]		LM5166 VSON 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits are based on T_J = –40°C to +125°C. V_{IN} = 12 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Q\text{-}SD}$	VIN DC supply current, shutdown	V_{EN} = 0 V, T_J = 25°C		4	6	µA
$I_{Q\text{-}SLEEP}$	VIN DC supply current, no load	V_{FB} = 1.5 V, T_J = 25°C		9.7	15	µA
$I_{Q\text{-}SLEEP\text{-}VINMAX}$	VIN DC supply current, no load, V_{VIN} = 65 V	V_{FB} = 1.5 V, V_{VIN} = 65 V, T_J = 25°C		10	15	µA
$I_{Q\text{-}ACTIVE\text{-}PFM}$	VIN DC supply current, active, max load	PFM mode, R_{RT} = 0 Ω, R_{SS} = 100 kΩ		205		µA
$I_{Q\text{-}ACTIVE\text{-}COT}$	VIN DC supply current, active, max load	COT mode, R_{RT} = R_{SS} = 100 kΩ		320		µA
POWER SWITCHES						
R_{DSON1}	High-side MOSFET $R_{DS(on)}$	I_{SW} = –100 mA		0.93		Ω
R_{DSON2}	Low-side MOSFET $R_{DS(on)}$	I_{SW} = 100 mA		0.48		Ω
CURRENT LIMITING						
I_{HS_LIM1}	High-side peak current limit thresholds	See Table 3	1125	1250	1375	mA
I_{HS_LIM2}			675	750	825	mA
I_{HS_LIM3}			440	500	560	mA
I_{LS_LIM1}	Low-side valley current limit thresholds	See Table 3		415		mA
I_{LS_LIM2}				315		mA
REGULATION COMPARATOR						
V_{VOUT5}	VOUT 5-V DC setpoint	LM5166X	4.9	5.0	5.1	V
$V_{VOUT3.3}$	VOUT 3.3-V DC setpoint	LM5166Y	3.23	3.30	3.37	V
I_{VOUT}	VOUT pin input current	V_{VOUT} = 5 V, LM5166X		7		µA
		V_{VOUT} = 3.3 V, LM5166Y		3.8		µA
V_{FB1}	Lower FB regulation threshold (PFM and COT)	Adjustable VOUT version	1.208	1.223	1.238	V
V_{FB2}	Upper FB regulation threshold (PFM)	Adjustable VOUT version	1.218	1.233	1.248	V
I_{FB}	FB pin input bias current	V_{FB} = 1 V			100	nA
$FB_{HYS\text{-}PFM}$	FB comparator PFM hysteresis	PFM mode		10		mV
$FB_{HYS\text{-}COT}$	FB comparator dropout hysteresis	COT mode		4		mV
$FB_{LINE\text{-}REG}$	FB threshold variation over line	V_{VIN} = 3 V to 65 V		0.005		%/V
$VOUT_{LINE\text{-}REG}$	VOUT threshold variation over line	LM5166X, V_{VIN} = 6 V to 65 V LM5166Y, V_{VIN} = 4.5 V to 65 V		0.005		%/V
POWER GOOD						
UVT_{RISING}	PGOOD comparator	V_{FB} rising relative to V_{FB1} threshold		94%		
$UVT_{FALLING}$	PGOOD comparator	V_{FB} falling relative to V_{FB1} threshold		87%		

Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits are based on T_J = –40°C to +125°C. V_{IN} = 12 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PGOOD}	PGOOD on-resistance	V_{FB} = 1 V		80	200	Ω
$V_{INMIN-PGOOD}$	Minimum required VIN for valid PGOOD	V_{VIN} falling I_{PGOOD} = 0.1 mA, V_{PGOOD} < 0.5 V		1.2	1.65	V
I_{PGOOD}	PGOOD off-state leakage	V_{FB} = 1.2 V, V_{PGOOD} = 5.5 V		10	100	nA
ENABLE / UVLO						
V_{IN-ON}	Turn-on threshold	V_{VIN} rising	2.60	2.75	2.95	V
V_{IN-OFF}	Turn-off threshold	V_{VIN} falling	2.35	2.45	2.60	V
V_{EN-ON}	EN turn-on threshold	V_{EN} rising	1.163	1.22	1.276	V
V_{EN-OFF}	EN turn-off threshold	V_{EN} falling	1.109	1.144	1.178	V
V_{EN-HYS}	EN hysteresis			76		mV
V_{EN-SD}	EN shutdown threshold	V_{EN} falling	0.3	0.6		V
R_{HYS}	HYS on-resistance	V_{EN} = 1 V		80	200	Ω
I_{HYS}	HYS off-state leakage	V_{EN} = 1.5 V, V_{HYS} = 5.5 V		10	100	nA
SOFT-START						
I_{SS}	Soft-start charging current	V_{SS} = 1 V		10		µA
T_{SS-INT}	Soft-start rise time	SS floating		900		µs
THERMAL SHUTDOWN						
T_{J-SD}	Thermal shutdown threshold			170		°C
$T_{J-SD-HYS}$	Thermal shutdown hysteresis			10		°C

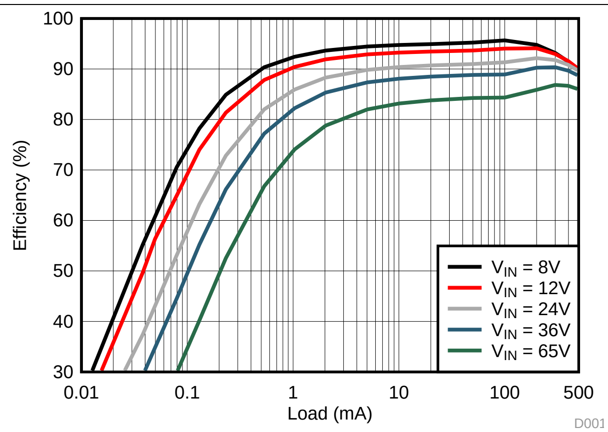
6.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{ON-MIN}	Minimum on-time			180		ns
T_{ON1}	On-time	16 kΩ from RT to GND		280		ns
T_{ON2}	On-time	75 kΩ from RT to GND		1150		ns

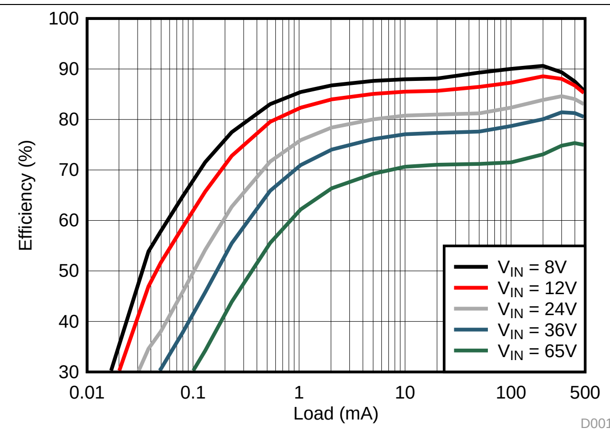
6.7 Typical Characteristics

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to Typical Applications for circuit designs.



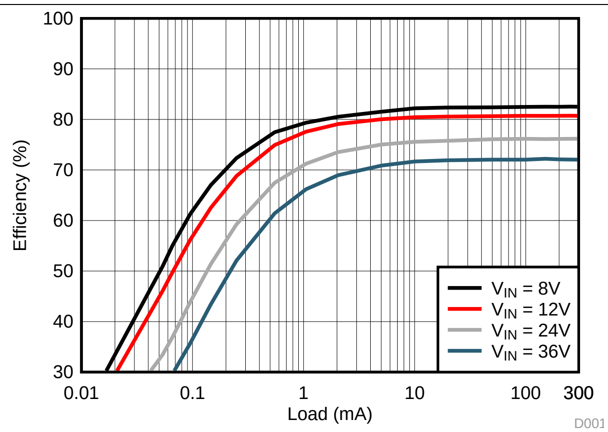
See schematic, Figure 50 | L_F = 150 µH, C_{OUT} = 47 µF | $F_{SW(nom)}$ = 100 kHz, R_{RT} = 309 kΩ

Figure 1. Converter Efficiency: 5 V, 500 mA, COT



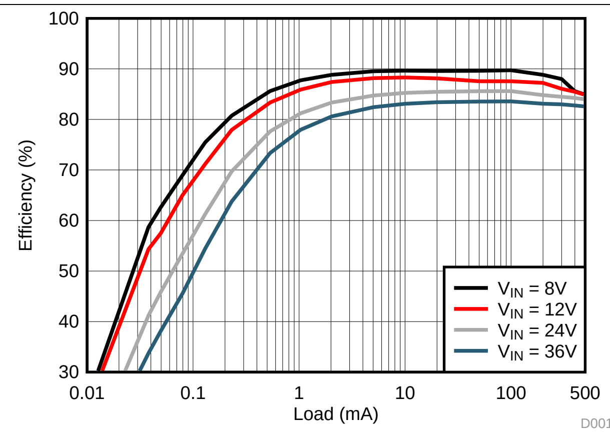
See schematic, Figure 61 | L_F = 47 µH, C_{OUT} = 47 µF | $F_{SW(nom)}$ = 200 kHz, R_{RT} = 100 kΩ

Figure 2. Converter Efficiency: 3.3 V, 500 mA, COT



See schematic, Figure 68 | L_F = 4.7 µH, C_{OUT} = 47 µF | $F_{SW(nom)}$ = 600 kHz, R_{RT} = 0 Ω

Figure 3. Converter Efficiency: 3.3 V, 300 mA, PFM



See schematic, Figure 75 | L_F = 22 µH, C_{OUT} = 200 µF | $F_{SW(nom)}$ = 100 kHz, R_{RT} = 0 Ω

Figure 4. Converter Efficiency: 5 V, 500 mA, PFM

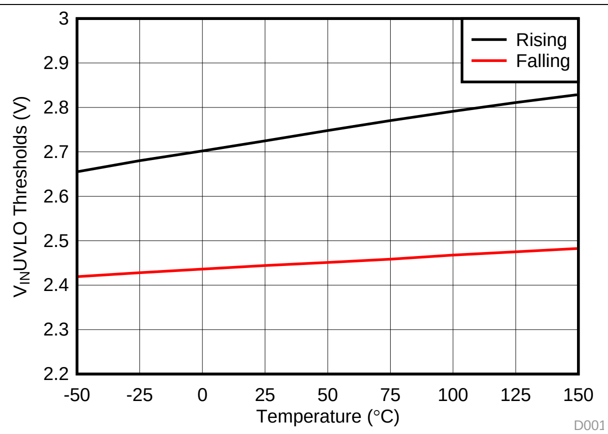


Figure 5. Internal V_{IN} UVLO Voltage vs Temperature

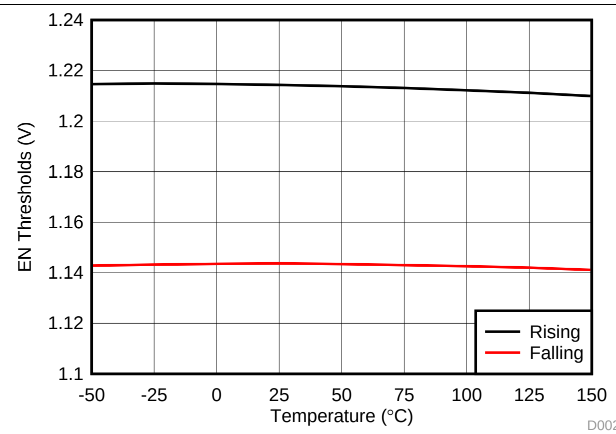


Figure 6. Enable Threshold Voltage vs Temperature

Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to Typical Applications for circuit designs.

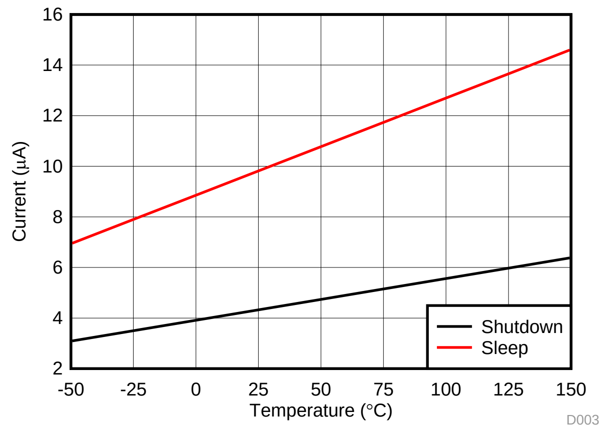


Figure 7. V_{IN} Sleep and Shutdown Supply Current vs Temperature

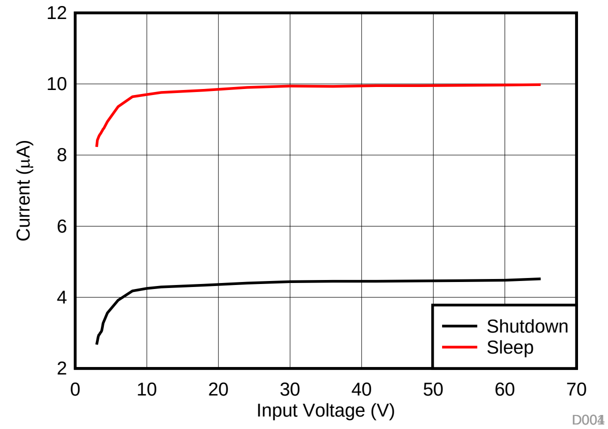


Figure 8. V_{IN} Sleep and Shutdown Supply Current vs Input Voltage

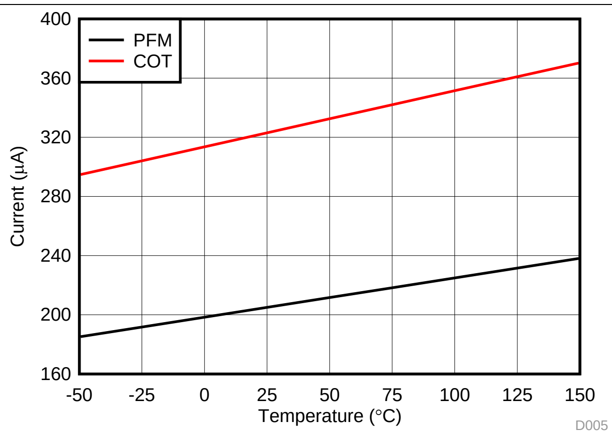


Figure 9. V_{IN} Active Mode Supply Current vs Temperature

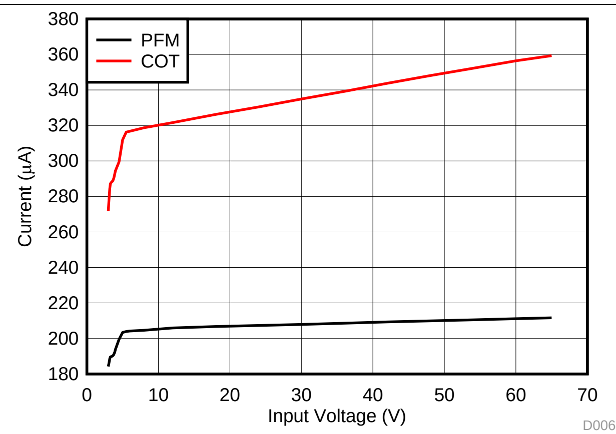


Figure 10. V_{IN} Active Mode Supply Current vs Input Voltage

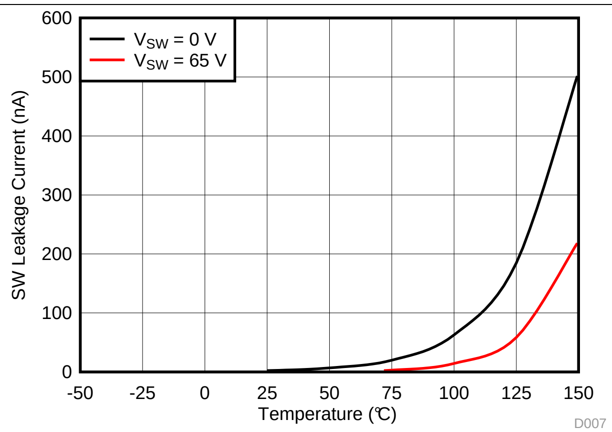


Figure 11. SW Pin Leakage Current vs Temperature V_{VIN} = 65 V

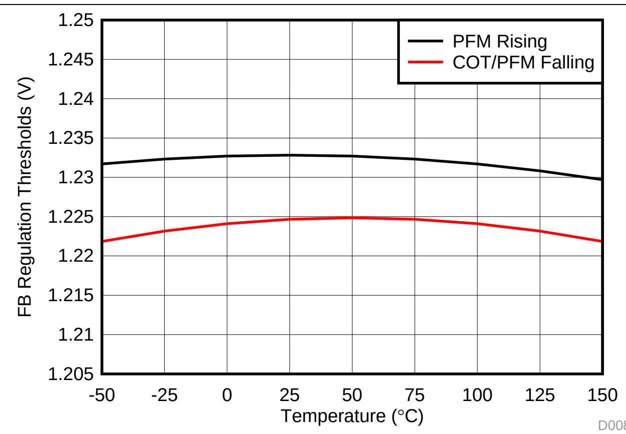


Figure 12. Feedback Comparator Threshold Voltage vs Temperature

Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to Typical Applications for circuit designs.

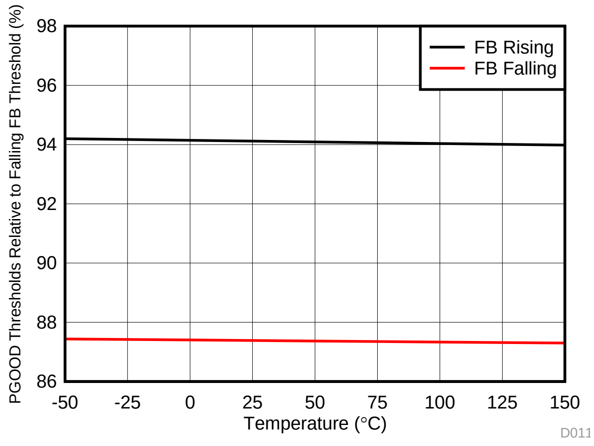


Figure 13. PGOOD Thresholds vs Temperature

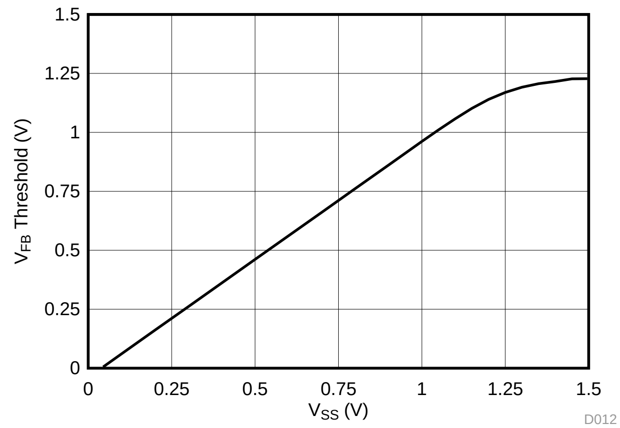


Figure 14. Feedback Voltage vs Soft-start Voltage

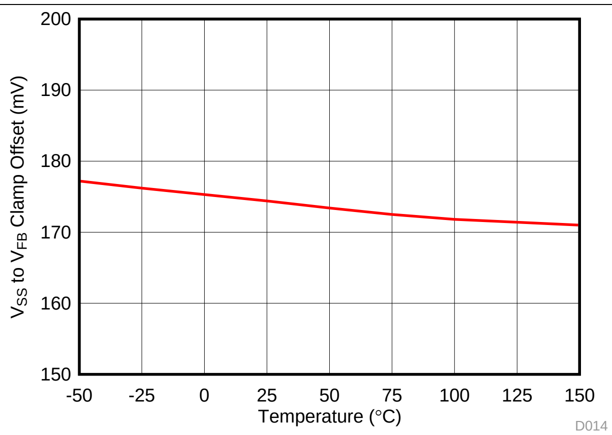


Figure 15. Soft-start to Feedback Clamp Offset vs Temperature

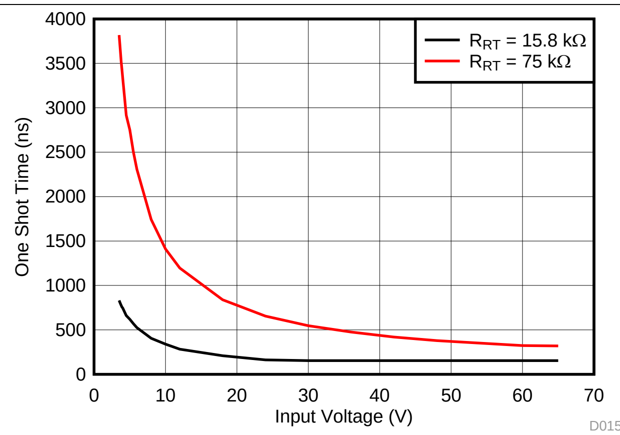


Figure 16. COT One-shot Timer T_{ON} vs Input Voltage

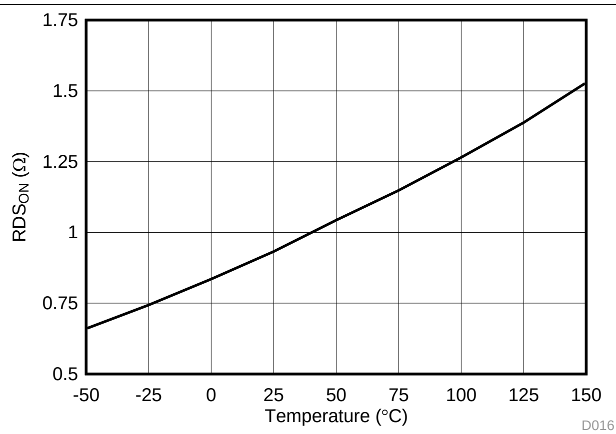


Figure 17. High-Side MOSFET On-state Resistance vs Temperature

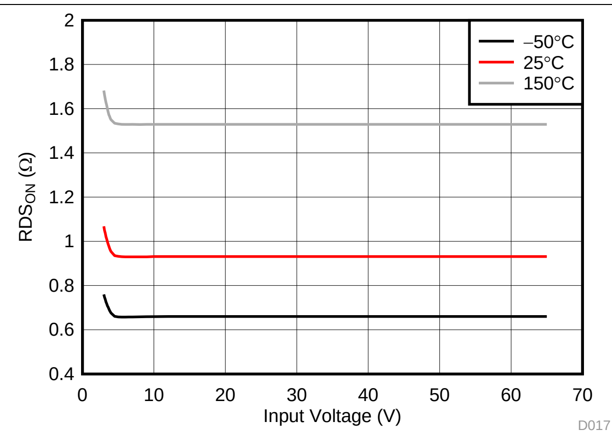


Figure 18. High-Side MOSFET On-state Resistance vs Input Voltage

Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to Typical Applications for circuit designs.

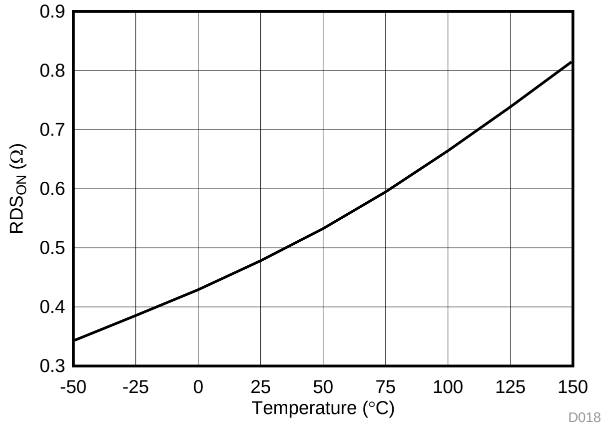


Figure 19. Low-Side MOSFET On-state Resistance vs Temperature

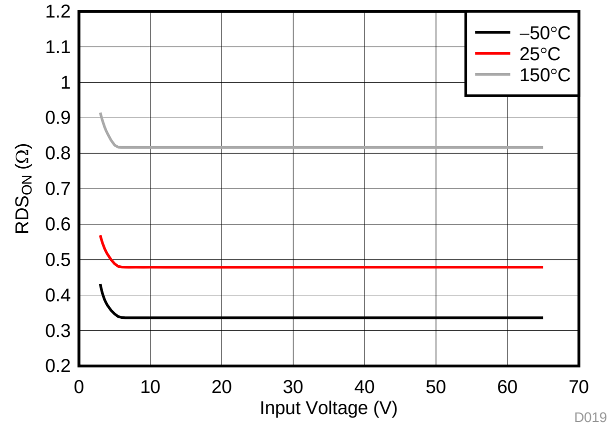


Figure 20. Low-Side MOSFET On-state Resistance vs Input Voltage

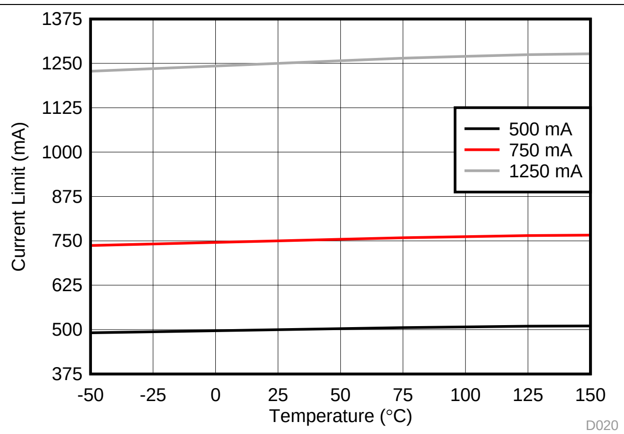


Figure 21. High-Side Peak Current Limit vs Temperature

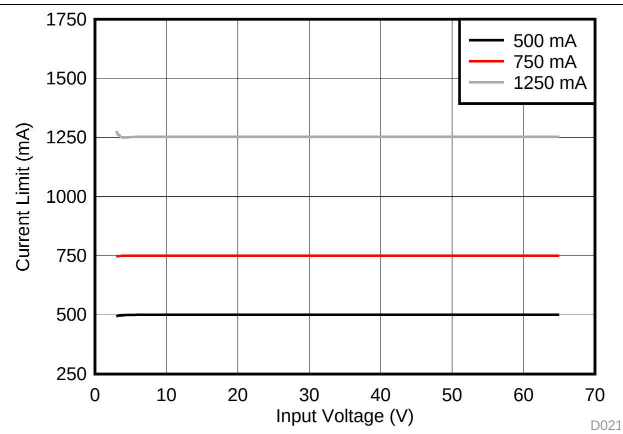


Figure 22. High-Side Peak Current Limit vs Input Voltage

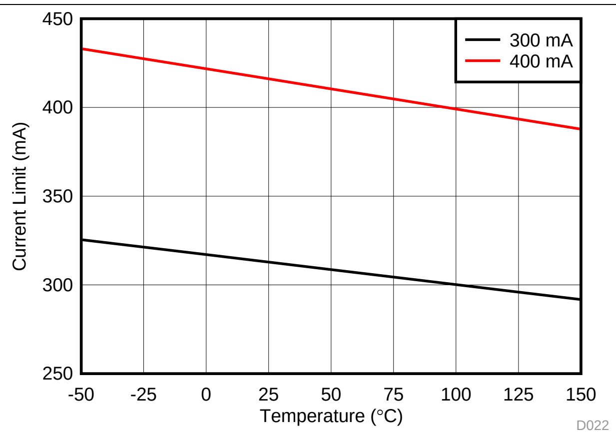


Figure 23. Low-Side Valley Current Limit vs Temperature

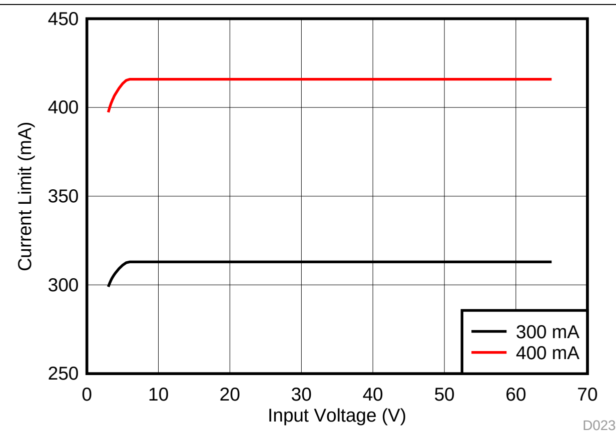


Figure 24. Low-Side Valley Current Limit vs Input Voltage

Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to Typical Applications for circuit designs.

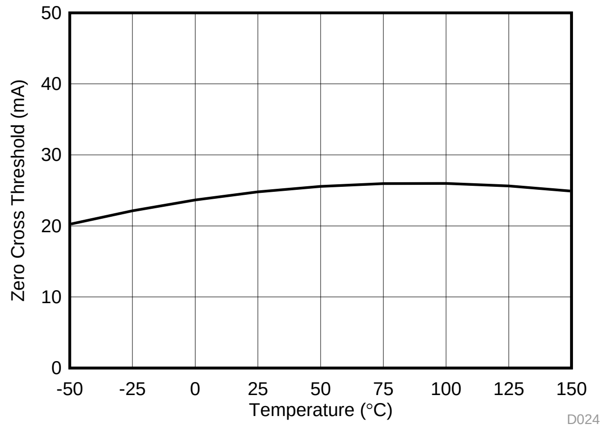


Figure 25. Zero-Cross Current Threshold vs Temperature

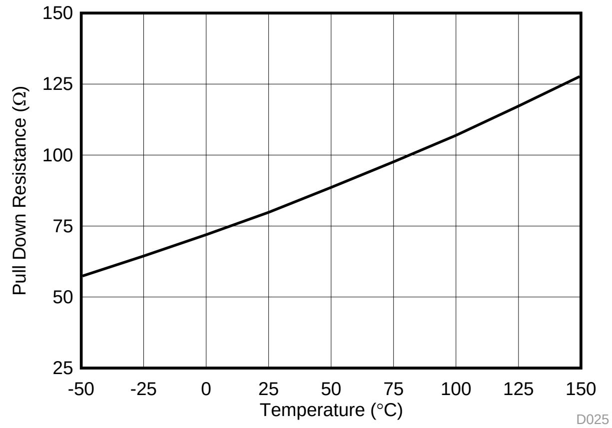
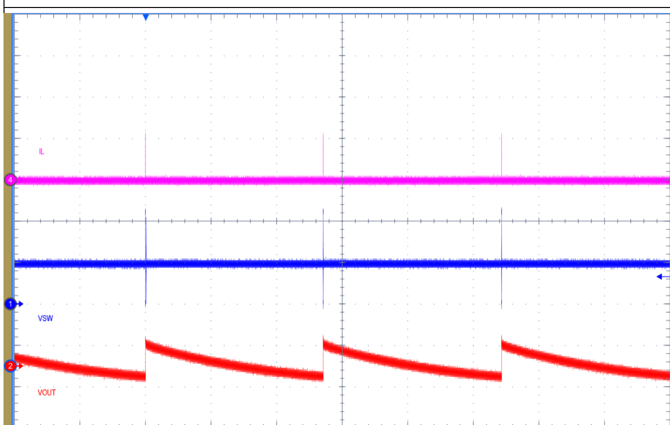
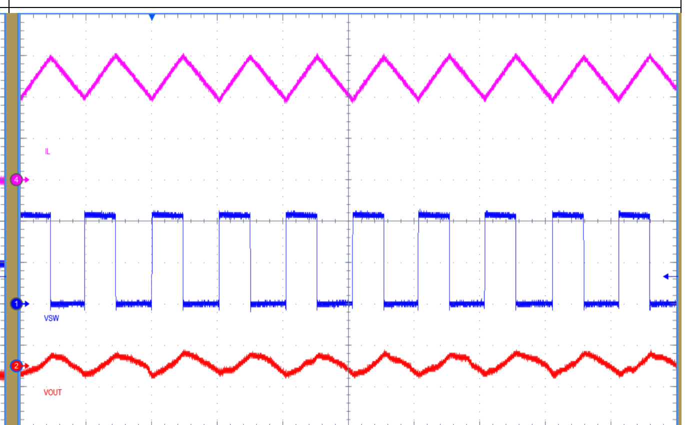


Figure 26. PGOOD and HYS Pull-down $R_{DS(on)}$ vs Temperature



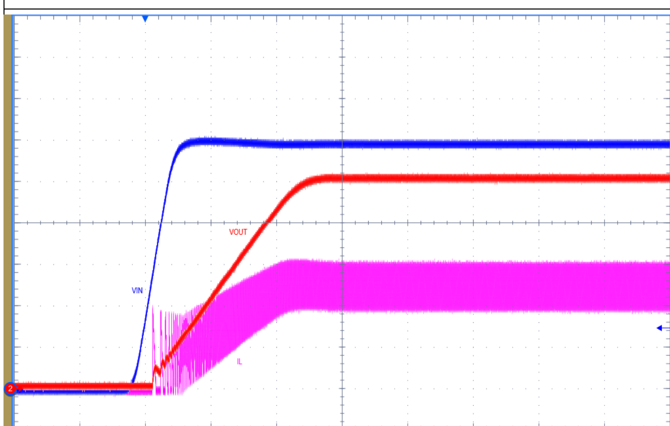
Time Scale: 20 ms/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 50 mV/Div
CH4: I_L, 200 mA/Div

Figure 27. No Load Switching Waveforms, COT, Type 2



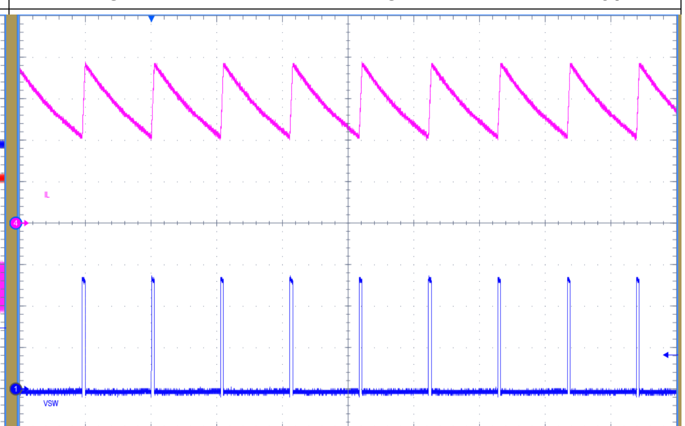
Time Scale: 10 µs/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 50 mV/Div
CH4: I_L, 200 mA/Div

Figure 28. Full Load Switching Waveforms, COT, Type 2



Time Scale: 2 ms/Div
CH1: V_{IN}, 2 V/Div
CH2: V_{OUT}, 1 V/Div
CH4: I_L, 200 mA/Div

Figure 29. Full Load Startup, COT, Type 2

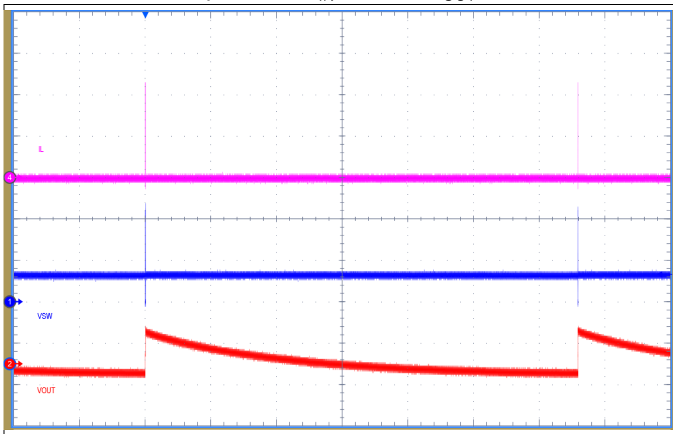


Time Scale: 100 µs/Div
CH1: V_{SW}, 4 V/Div
CH4: I_L, 200 mA/Div

Figure 30. Short Circuit, COT, Type 2

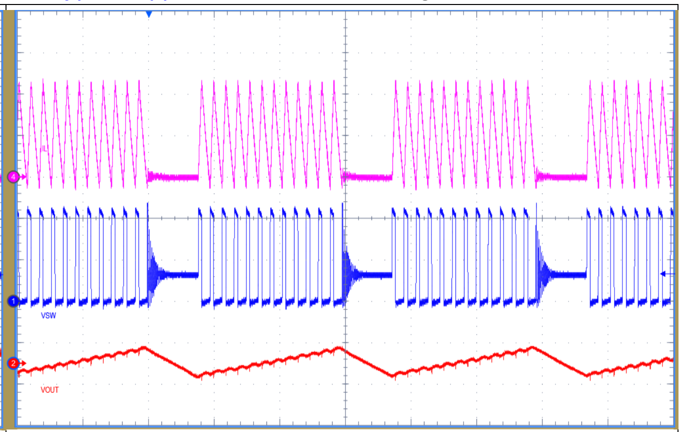
Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to Typical Applications for circuit designs.



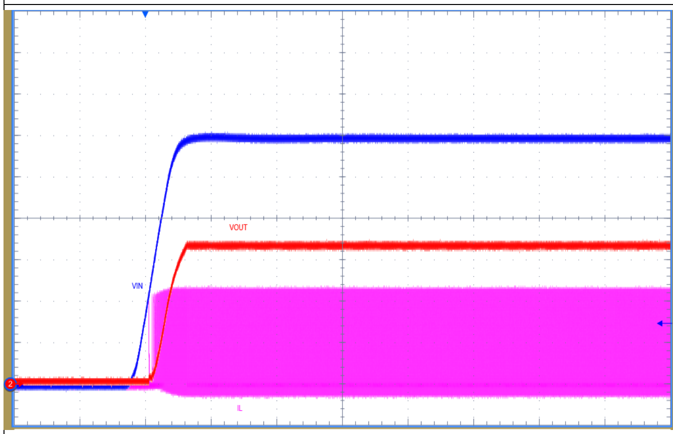
Time Scale: 20 ms/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 50 mV/Div
CH4: I_L, 400 mA/Div

Figure 31. No Load Switching Waveforms PFM Mode, I_{LIM} = 750 mA



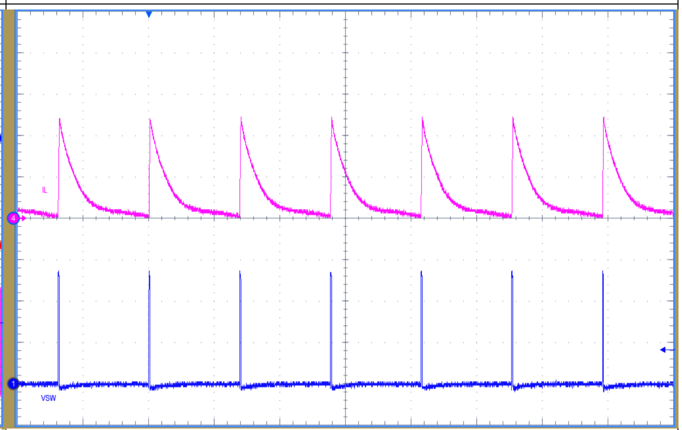
Time Scale: 10 µs/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 100 mV/Div
CH4: I_L, 400 mA/Div

Figure 32. Full Load Switching Waveforms PFM Mode, I_{LIM} = 750 mA



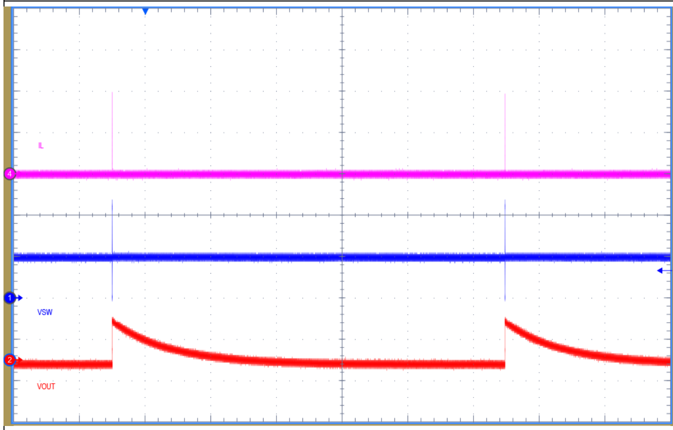
Time Scale: 2 ms/Div
CH1: V_{IN}, 2 V/Div
CH2: V_{OUT}, 1 V/Div
CH4: I_L, 400 mA/Div

Figure 33. Full Load Startup, PFM, I_{LIM} = 750 mA



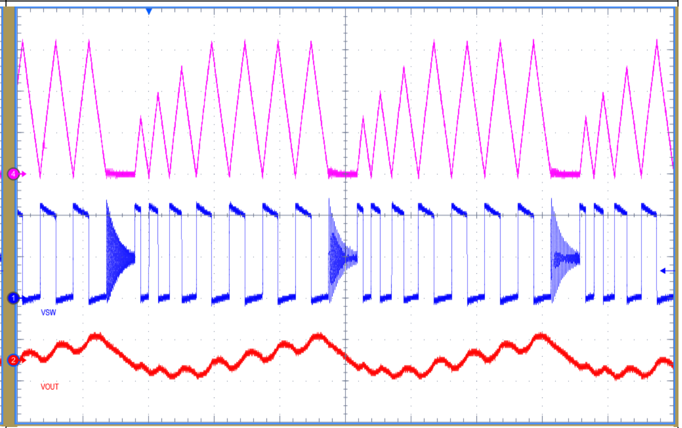
Time Scale: 20 µs/Div
CH1: V_{SW}, 4 V/Div
CH4: I_L, 400 mA/Div

Figure 34. Short Circuit, PFM, I_{LIM} = 750 mA



Time Scale: 50 ms/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 50 mV/Div
CH4: I_L, 400 mA/Div

Figure 35. No Load Switching Waveforms PFM Mode, I_{LIM} = 1.25 A, Modulated



Time Scale: 20 µs/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 100 mV/Div
CH4: I_L, 400 mA/Div

Figure 36. Full Load Switching Waveforms PFM Mode, I_{LIM} = 1.25 A, Modulated

7 Detailed Description

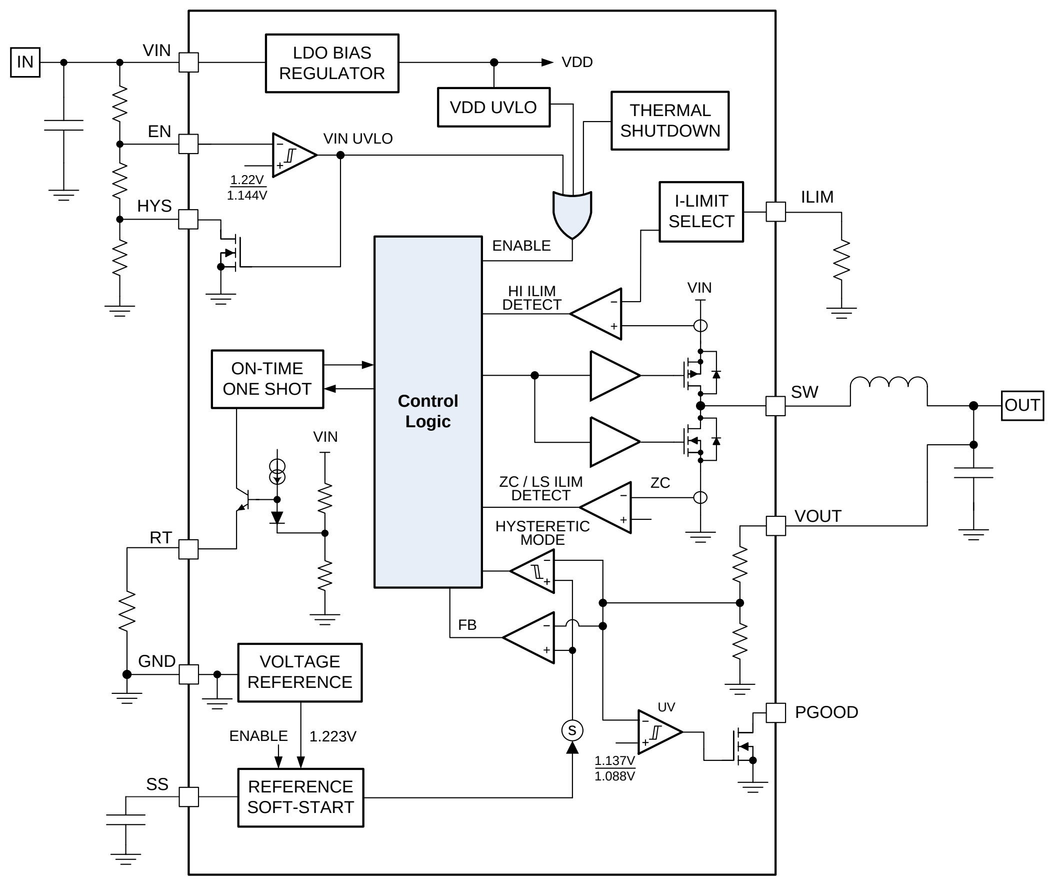
7.1 Overview

The LM5166 regulator is an easy-to-use synchronous buck DC/DC converter that operates from a 3-V to 65-V supply voltage. The device is intended for step-down conversions from 5-V, 12-V, 24-V, and 48-V unregulated, semi-regulated and fully-regulated supply rails. With integrated high-side and low-side power MOSFETs, the LM5166 delivers up to 500-mA DC load current with exceptional efficiency and ultra-low input quiescent current in a very small solution size.

Designed for simple implementation, a choice of operating modes offers flexibility to optimize its usage according to the target application. Fixed-frequency, constant on-time (COT) operation with discontinuous conduction mode (DCM) at light loads is ideal for low-noise, high current, fast transient load requirements. Alternatively, pulse frequency modulation (PFM) mode achieves ultra-high light-load efficiency performance. Control loop compensation is not required with either operating mode which reduces design time and external component count.

The LM5166 incorporates other features for comprehensive system requirements, including an open-drain Power Good circuit for power-rail sequencing and fault reporting, internally-fixed or externally-adjustable soft-start, monotonic startup into pre-biased loads, precision enable with customizable hysteresis for programmable line undervoltage lockout (UVLO), and thermal shutdown with automatic recovery. These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for simple and optimized PCB layout, requiring only a few external components.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Integrated Power MOSFETs

The LM5166 is a step-down buck converter with integrated high-side PMOS buck switch and low-side NMOS synchronous switch. During the high-side MOSFET on-time, the SW voltage V_{SW} swings up to approximately V_{IN}, and the inductor current increases with slope $(V_{IN} – V_{OUT})/L_F$. When the high-side MOSFET is turned off by the control logic, the low-side MOSFET turns on after a fixed deadtime. Inductor current flows through the low-side MOSFET with slope $–V_{OUT}/L_F$. Duty cycle D is defined as T_{ON}/T_{SW}, where T_{ON} is the high-side MOSFET conduction time and T_{SW} is the switching period.

7.3.2 Selectable PFM or COT Mode Converter Operation

Depending on how the RT pin is connected, the LM5166 operates in PFM or COT mode. With the RT pin tied to GND, the device operates in PFM mode. An R_{RT} resistor connected between the RT and GND pins enables COT control and sets the desired switching frequency as defined by Equation 4. Figure 37 and Figure 38 show converter schematics for PFM and COT modes of operation.

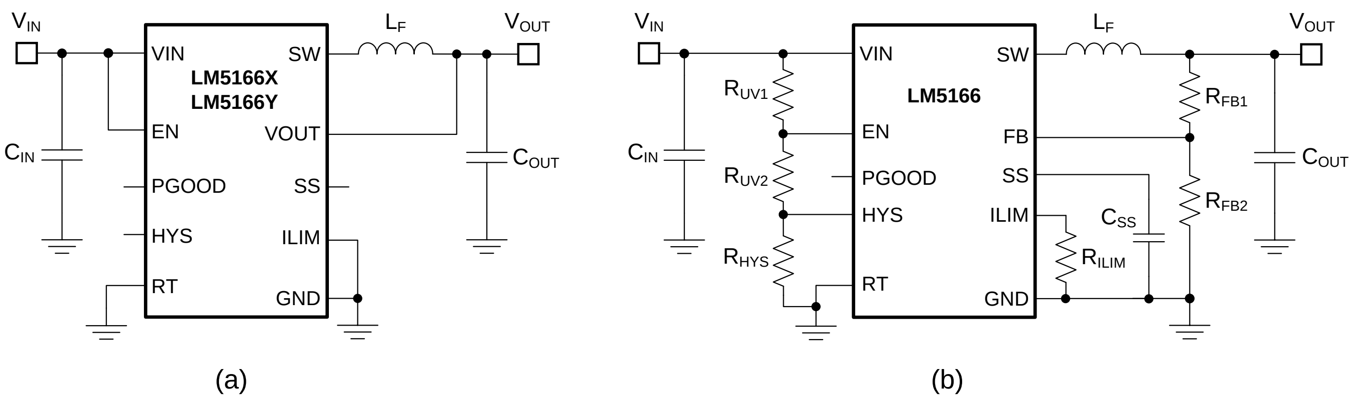


Figure 37. PFM Mode Converter Schematics: (a) Fixed Output Voltage of 5 V or 3.3 V, (b) Adjustable Output Voltage With Programmable Soft Start, Current Limit and UVLO

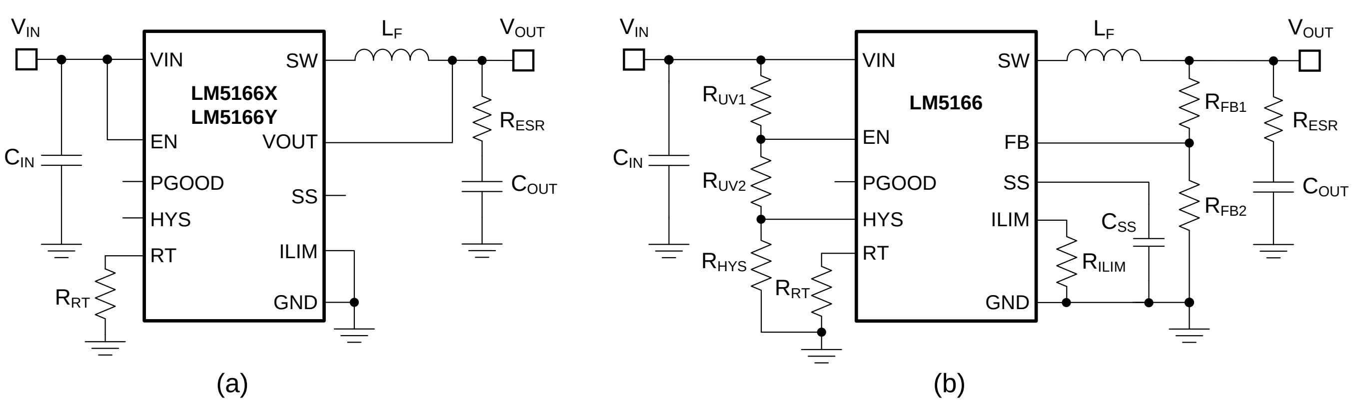


Figure 38. COT Mode Converter Schematics: (a) Fixed Output Voltage of 5 V or 3.3 V, (b) Adjustable Output Voltage With Programmable Soft Start, Current Limit and UVLO

Feature Description (continued)

7.3.2.1 PFM Mode Operation

In PFM mode, the LM5166 behaves as a hysteretic voltage regulator operating in boundary conduction mode. The output voltage is regulated between upper and lower threshold levels according to the PFM feedback comparator hysteresis of 10 mV. Figure 39 shows the relevant output voltage and inductor current waveforms. The LM5166 provides the required switching pulses to recharge the output capacitor to the upper threshold, followed by a sleep period where most of the internal circuits are disabled. The load current is supported by the output capacitor during this time, and the LM5166 current consumption reduces to 9.7 µA. The sleep period duration depends on load current and output capacitance.

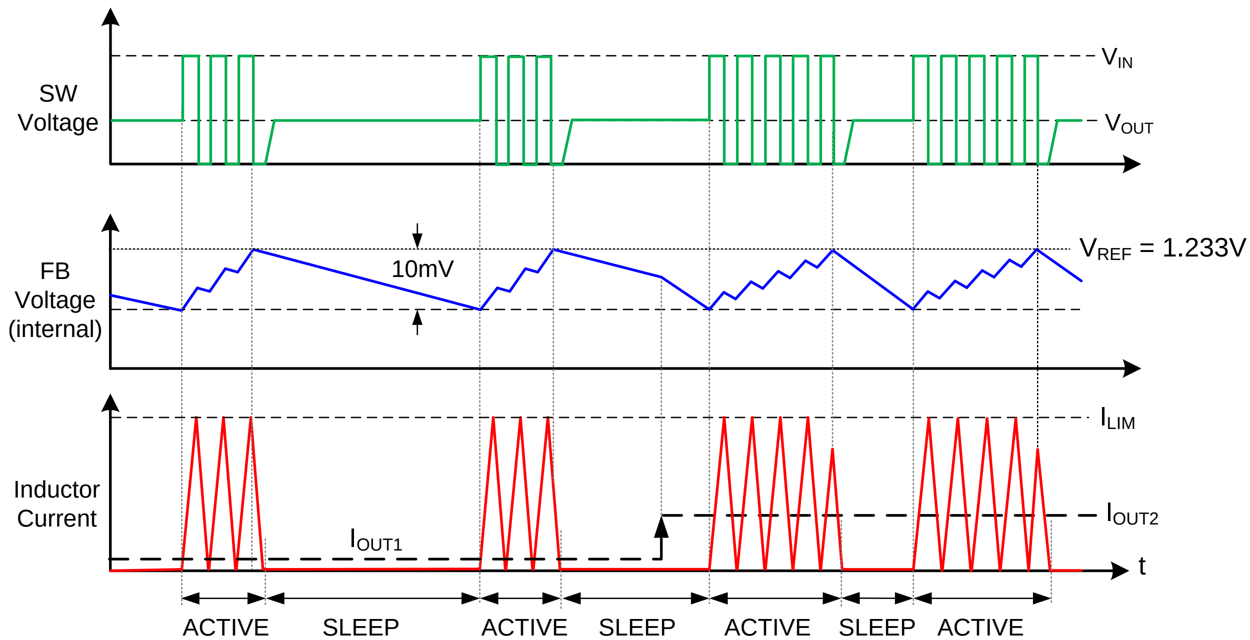


Figure 39. PFM Mode Output Voltage and Inductor Current Waveforms

When operating in PFM mode at given input and output voltages, the chosen filter inductance dictates the PFM pulse frequency as

$$F_{SW(PFM)} = \frac{V_{OUT}}{L_F \cdot I_{PK(PFM)}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

where $I_{PK(PFM)}$ is one of the programmable levels for peak current limit. See Adjustable Current Limit for more detail.

One of the supported ILIM settings enables a function that modulates the peak current threshold levels during the first three switching cycles of each active period as illustrated in Figure 40. This function improves efficiency under most application conditions at the expense of slightly degraded transient load response.

Feature Description (continued)

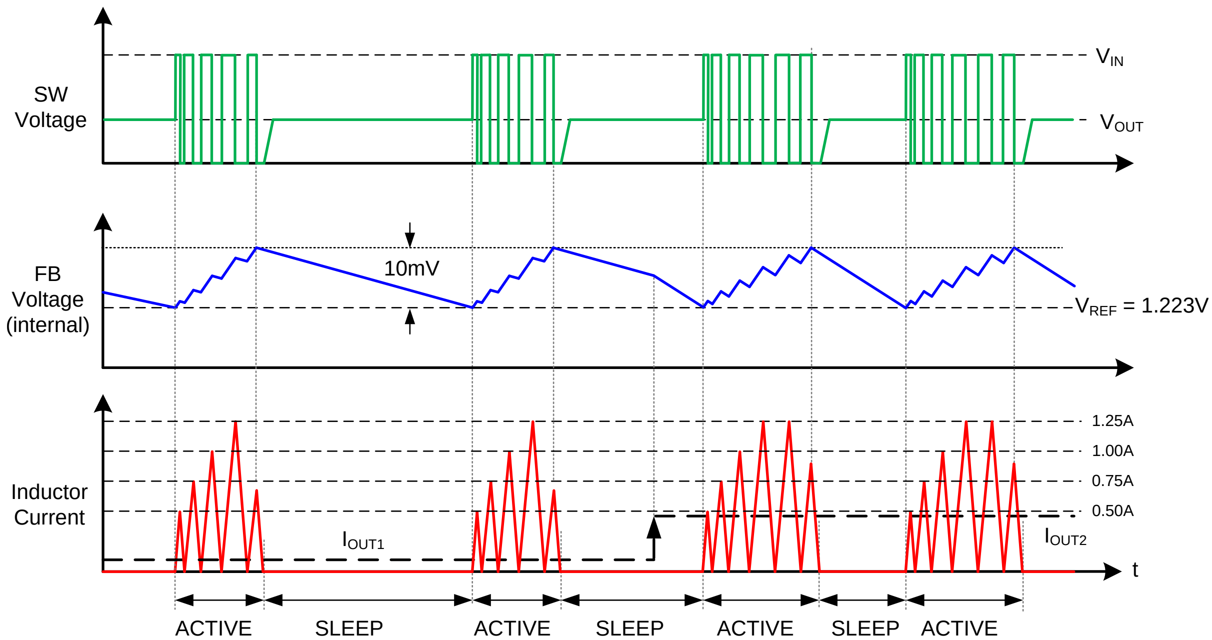


Figure 40. PFM Mode with Modulated I_{LIM} Output Voltage and Inductor Current Waveforms

As expected, the choice of mode and switching frequency represents a compromise between conversion efficiency, quiescent current, and passive component size. Lower switching frequency implies reduced switching losses (including gate charge losses, transition losses, etc.) and higher overall efficiency. Higher switching frequency, on the other hand, implies smaller LC output filter and hence, a more compact design. Lower inductance also helps transient response and reduces the inductor DCR conduction loss. The ideal switching frequency in a given application is a tradeoff and thus is determined on a case-by-case basis. It relates to the input voltage, output voltage, most frequent load current level(s), external component choices, and circuit size requirement. At light loads, the PFM converter has a relatively longer sleep time interval and thus operates at lower input quiescent current levels.

7.3.2.2 COT Mode Operation

In COT mode, the LM5166-based converter turns on the high-side MOSFET with constant on-time that adapts to V_{IN}, as defined by Equation 2, to operate with nearly fixed switching frequency when in continuous conduction mode (CCM). The high-side MOSFET turns on when the feedback voltage (V_{FB}) falls below the reference voltage. The regulator control loop maintains a constant output voltage by adjusting the PWM off-time as defined with Equation 3. For stable operation, the feedback voltage must decrease monotonically in phase with the inductor current during the off-time as explained in Ripple Generation Methods.

$$t_{ON}[ns] = \frac{175 \cdot R_{RT}[k\Omega]}{V_{IN}} \tag{2}$$

$$t_{OFF} = \frac{L_F \cdot \Delta I_{L(nom)}}{V_{OUT} + (R_{DCR} + R_{DSON1}) \cdot I_{OUT}} \tag{3}$$

Diode emulation mode (DEM) prevents negative inductor current, and pulse skipping maintains high efficiency at light load currents by decreasing the effective switching frequency. The COT-controlled LM5166 waveforms in CCM and DEM are shown in Figure 41.

Feature Description (continued)

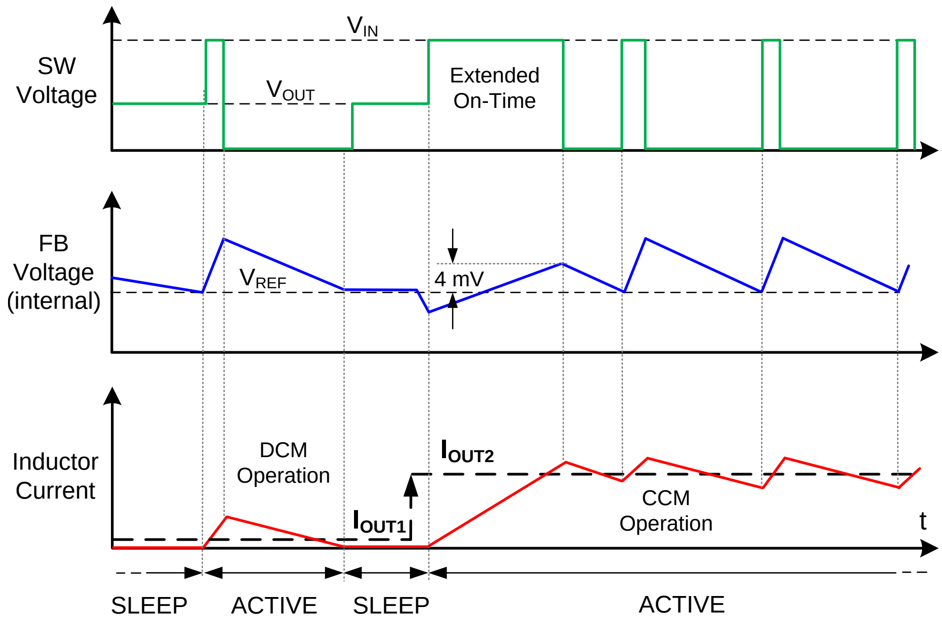


Figure 41. COT Mode Feedback Voltage and Inductor Current Waveforms

The required on-time adjust resistance for a particular frequency (in CCM) is given in Equation 4 and tabulated in Table 1. The maximum programmable on-time is 15 µs.

$$R_{RT}[k\Omega] = \frac{V_{OUT}[V]}{F_{SW}[kHz]} \cdot \frac{10^4}{1.75} \tag{4}$$

Table 1. On-Time Adjust Resistance (E96 EIA Values) for Various Switching Frequencies and Output Voltages(1)

F_{SW} (kHz)	R_{RT} (kΩ)			
	V_{OUT} = 1.8 V	V_{OUT} = 3.3 V	V_{OUT} = 5 V	V_{OUT} = 12 V
100	102	187	287	681
200	51.1	95.3	143	340
300	34	63.4	95.3	226
400	25.5	47.5	71.5	169
500	20.5	37.4	57.6	137
600	16.9	31.6	47.5	115

(1) For a more precise adjustment of the switching frequency consider Equation 2 and Equation 3. The *LM5166 Quick-Start Design Tool* estimates and plots the switching frequency as a function of the load current.

7.3.2.2.1 Ripple Generation Methods

In the Constant-On-Time (COT) control scheme, the on-time is terminated by a one-shot, and the off-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage (V_{FB1}). Therefore, for stable operation, the feedback voltage must decrease monotonically in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage (V_{FB}) during off-time must be large enough to dominate any noise present at the feedback node.

Table 2 presents three different methods for generating appropriate voltage ripple at the feedback node. Type 1 ripple generation method uses a single R_{ESR} resistor in series with the output capacitor. The generated voltage ripple has two components:

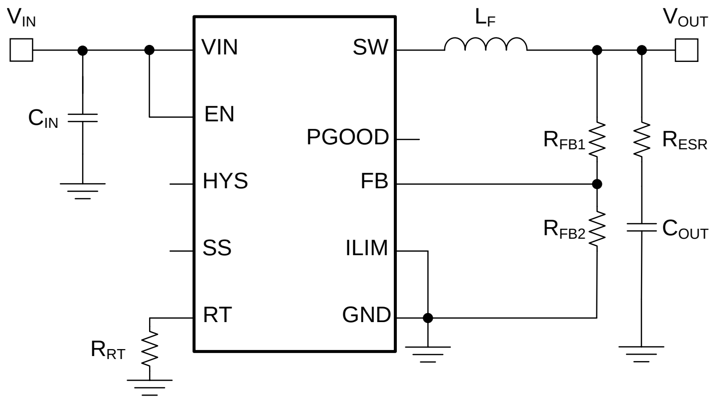
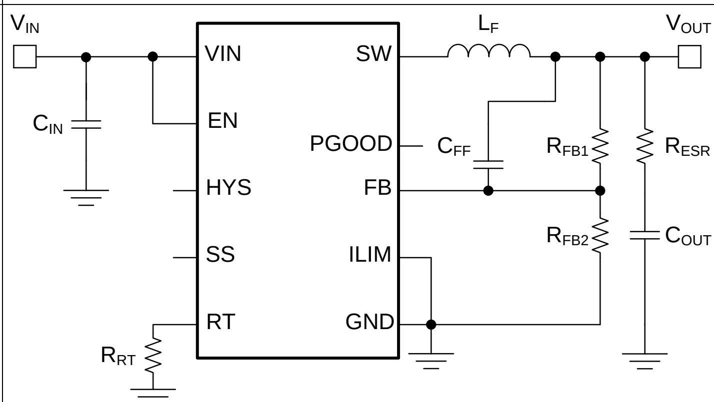
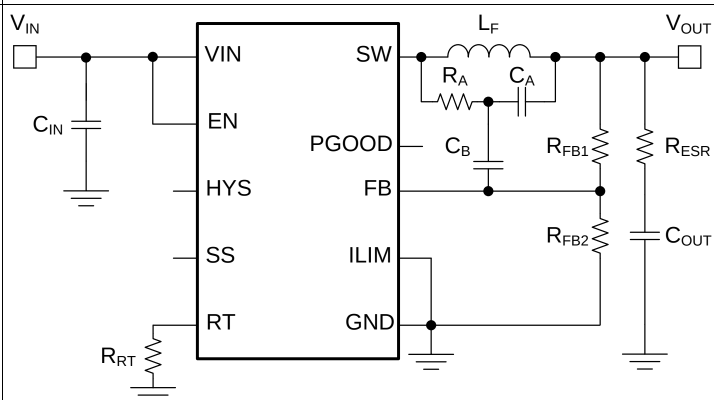
- Capacitive ripple caused by the inductor current ripple charging/discharging the output capacitor.
- Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor and R_{ESR}

The capacitive ripple component is out of phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple component is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at the output (V_{OUT}) for stable operation. If this condition is not satisfied unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off-time. Equation 5 and Equation 6 define the value of the R_{ESR} resistor that ensures required amplitude and phase of the ripple at the feedback node.

Type 2 ripple generation method uses a C_{FF} capacitor in addition to the R_{ESR} resistor. As the output voltage ripple is directly AC-coupled by C_{FF} to the feedback node, the R_{ESR} value and ultimately the output voltage ripple are reduced by a factor of V_{OUT} / V_{FB1}.

Type 3 ripple generation method uses an RC network consisting of R_A and C_A, and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is then AC-coupled into the feedback node (FB) with the capacitor C_B. Since this circuit does not use the output voltage ripple, it is suited for applications where low output voltage ripple is critical. Application note AN-1481 provides additional details on this topic.

Table 2. Ripple Generation Methods

Type 1 Lowest Cost		$R_{ESR} \geq \frac{20mV \cdot V_{OUT}}{V_{FB1} \cdot \Delta I_{L(nom)}}$ (5) $R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}}$ (6)
Type 2 Reduced Ripple		$R_{ESR} \geq \frac{20mV}{\Delta I_{L(nom)}}$ (7) $R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}}$ (8) $C_{FF} \geq \frac{1}{2\pi \cdot F_{SW} \cdot (R_{FB1} \parallel R_{FB2})}$ (9)
Type 3 Lowest Ripple		$C_A \geq \frac{5}{F_{SW} \cdot (R_{FB1} \parallel R_{FB2})}$ (10) $R_A C_A \leq \frac{(V_{IN} - V_{OUT}) \cdot t_{ON(@V_{IN})}}{20mV}$ (11) $C_B \geq \frac{1}{2\pi \cdot F_{SW} \cdot (R_{FB1} \parallel R_{FB2})}$ (12)

7.3.2.2.2 COT Mode Light-Load Operation

Diode emulation mode (DEM) operation occurs when the low-side MOSFET switches off as the inductor valley current reaches zero. Here, the load current is less than half of the peak-to-peak inductor current ripple in CCM. Turning off the low-side MOSFET at zero current reduces switching loss, and preventing negative current conduction reduces conduction loss. In DEM, the duration that both high-side and low-side MOSFETs remain off progressively increases as load current decreases.

7.3.3 Low Dropout Operation and 100% Duty Cycle Mode

Using R_{DSON1} and R_{DSON2} for the high-side and low-side MOSFET on-state resistances, respectively, and R_{DCR} for the inductor DC resistance, the duty cycle in COT (CCM) or PFM mode is given by Equation 13.

$$D = \frac{V_{OUT} + \left(R_{DSON2} + R_{DCR}\right) \cdot I_{OUT}}{V_{IN} - \left(R_{DSON1} - R_{DSON2}\right) \cdot I_{OUT}} \approx \frac{V_{OUT}}{V_{IN}} \tag{13}$$

The LM5166 provides a low input voltage to output voltage dropout by engaging the high-side MOSFET at 100% duty cycle. In COT operation, the extended on-time mode seamlessly increases the duty cycle during low dropout conditions or load-step transients. The buck switch on-time extends based on the requirement that the FB voltage exceeds the internal 4-mV FB comparator hysteresis during any COT mode on-time. The on-time (and duty cycle) are extended as needed at low input voltage conditions until the FB voltage reaches the upper threshold. 100% duty cycle operation is eventually reached as the input voltage decreases to a level near the output setpoint. Very low dropout voltages can be achieved with 100% duty cycle and a low DCR inductor.

Note that PFM mode operation provides a natural transition to 100% duty cycle if needed during low input voltage conditions. If the input to output voltage difference is very low, the inductor current will increase to a level determined by the load and not reach the peak current threshold required to turn off the buck switch.

Use Equation 14 to calculate the minimum input voltage to maintain output regulation at 100% duty cycle.

$$V_{IN(min)} = V_{OUT} + I_{OUT} \cdot \left(R_{DSON1} + R_{DCR}\right) \tag{14}$$

7.3.4 Adjustable Output Voltage (FB)

Three voltage feedback settings are available: The fixed 3.3-V and 5-V versions include internal feedback resistors that sense the output directly through the VOUT pin; the adjustable voltage option senses the output through an external resistor divider connected from the output to the FB pin.

The LM5166 voltage regulation loop regulates the output voltage by maintaining the FB voltage equal to the internal reference voltage (V_{FB1}). A resistor divider programs the ratio from output voltage V_{OUT} to FB. For a target V_{OUT} setpoint, calculate R_{FB2} based on the selected R_{FB1} by

$$R_{FB2} = \frac{1.223\text{V}}{V_{OUT} - 1.223\text{V}} \cdot R_{FB1} \tag{15}$$

R_{FB1} in the range of 100 kΩ to 1 MΩ is recommended for most applications. A larger R_{FB1} consumes less DC current, which is necessary if light load efficiency is critical. However, R_{FB1} larger than 1 MΩ is not recommended as the feedback path becomes more susceptible to noise. Larger feedback resistances generally require more careful feedback path PCB layout. It is important to route the feedback trace away from the noisy area of the PCB. For more layout recommendations, please refer to PCB Layout .

7.3.5 Adjustable Current Limit

The LM5166 protects the system from overload conditions using cycle-by-cycle current limiting of the peak inductor current. The current sensed in the high-side MOSFET is compared to the current limit threshold set by the ILIM pin (See Table 3). Current is sensed after a 120-ns leading-edge blanking time following the high-side MOSFET turn on. The propagation delay of the current limit comparator is 80 ns, typical.

Table 3. Current Limit Thresholds

Mode of Operation	R_{ILIM} (kΩ)	Typical I_{HS_LIM} (mA)	Typical I_{LS_LIM} (mA)	I_{OUT_MAX} (mA)
COT Mode	0	750	415	500
	≥ 100(1)	500	315	300
PFM Mode	0	1250	N/A	500
	24.9	1250(2)	N/A	500
	56.2	750	N/A	300
	≥ 100(1)	500	N/A	200

(1) For this current limit threshold selection, the ILIM pin may also be left open instead of using a 100 kΩ or greater resistor.
(2) This I_{LIM} setting enables a function that modulates the I_{LIM} levels during the first three switching cycles as illustrated in Figure 40.

Note that in PFM mode, the inductor current ramps from zero to the chosen peak threshold every switching cycle. Consequently, the maximum output current is equal to half the peak inductor current. The output current capability in COT mode is higher and equal to the peak current threshold minus one-half the inductor ripple current. The ripple current is determined by the input and output voltage and the chosen inductance and frequency.

7.3.6 Precision Enable (EN) and Hysteresis (HYS)

The precision EN input supports adjustable input undervoltage lockout (UVLO) with hysteresis programmed independently via the HYS pin for application specific power-up and power-down requirements. EN connects to the input of a comparator with 76-mV hysteresis. The reference input of the comparator is connected to a 1.22-V bandgap reference. An external logic signal can be used to drive EN input to toggle the output on and off for system sequencing or protection. The simplest way to enable operation is to connect EN directly to VIN. This allows self-start-up of the LM5166 when V_{IN} is within its valid operating range. However, many applications benefit from using a resistor divider R_{UV1} and R_{UV2} as shown in Figure 42 to establish a precision UVLO level. Adding R_{HYS} and the connection to the HYS pin increases the voltage hysteresis as needed.

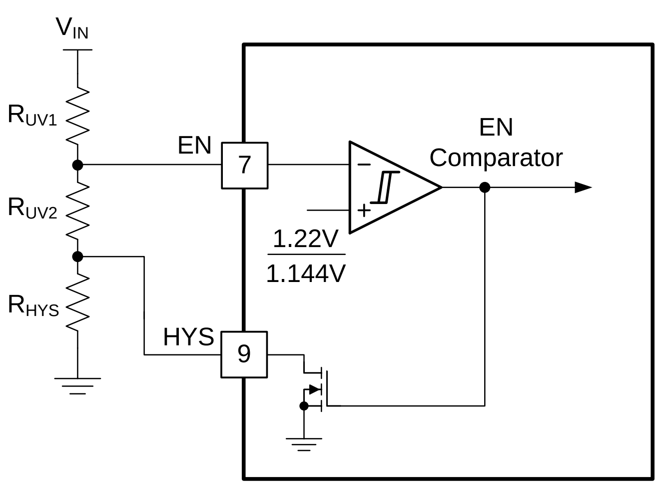


Figure 42. Input Voltage UVLO using EN and HYS

The input UVLO voltages are calculated using Equation 16 and Equation 17.

$$V_{IN(on)} = 1.22V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) \quad (16)$$

$$V_{IN(off)} = 1.144V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2} + R_{HYS}}\right) \quad (17)$$

The LM5166 enters a low I_Q shutdown mode when EN is pulled below an NPN transistor base-emitter voltage drop (approximately 0.6 V at room temperature). If EN is below this hard shutdown threshold, the internal LDO regulator powers off and the internal bias supply rail collapses, turning off the bias currents of the LM5166.

7.3.7 Power Good (PGOOD)

The LM5166 has a built-in PGOOD flag to indicate whether the output voltage is within a regulation window. The PGOOD signal can be used for startup sequencing of downstream converters, as shown in Figure 43, or fault protection. PGOOD is an open-drain output that requires a pullup resistor to a DC supply (12 V maximum). Typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the PGOOD pin voltage from a higher pullup rail.

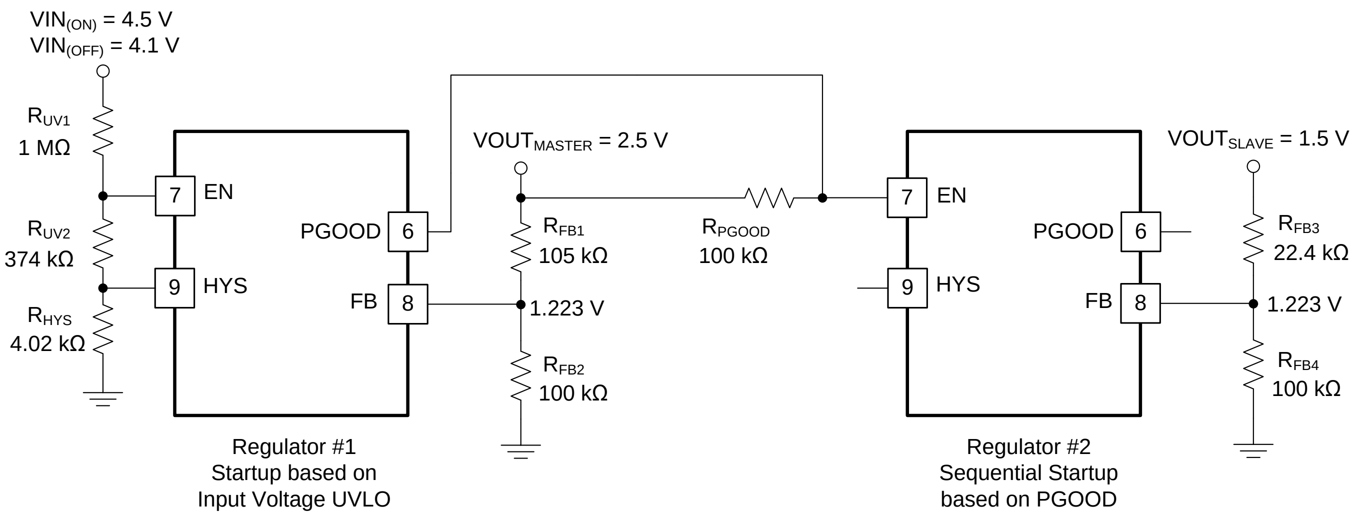


Figure 43. Master-Slave Sequencing Implementation Using PGOOD and EN

When the FB voltage exceeds 94% of the internal reference V_{FB1}, the PGOOD switch turns off and PGOOD will be pulled high. If the FB voltage falls below 87% of V_{FB1}, the PGOOD switch turns on, and PGOOD pulls low to indicate "power bad." The rising edge of PGOOD has a built-in noise filter delay of 5 µs.

7.3.8 Configurable Soft-Start (SS)

The LM5166 has a flexible and easy-to-use startup control through the SS pin. A soft-start feature prevents inrush current impacting the LM5166 and its supply when power is first applied. Soft-start is achieved by slowly ramping up the target regulation voltage when the device is enabled or powered up. Selectable/adjustable soft-start timing options include minimum delay (no soft-start), 900-µs internally fixed soft-start, and an externally-adjustable soft-start.

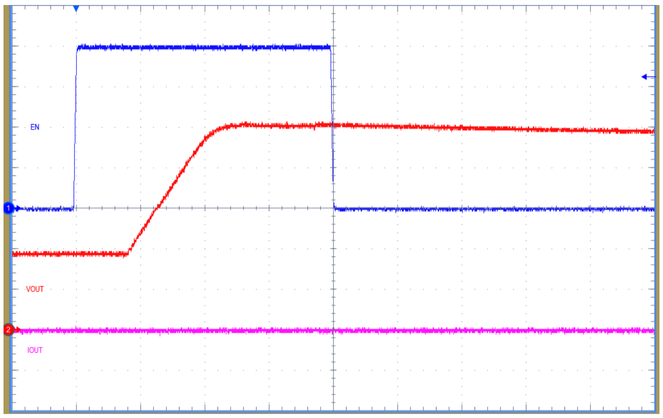
The simplest way to use the LM5166 is to leave the SS pin open circuit for a 900-µs soft-start time. The LM5166 will employ the internal soft-start control ramp and startup to the regulated output voltage. In applications with a large amount of output capacitors, higher V_{OUT}, or other special requirements, extend the soft-start time by connecting an external capacitor C_{SS} from SS to GND. Longer soft-start time further reduces the supply current needed to charge the output capacitors. An internal current source (I_{SS} = 10 µA) charges C_{SS} and generates a ramp to control the ramp rate of the output voltage. For a desired soft-start time t_{SS}, the C_{SS} capacitance is

$$C_{SS}[nF] = 8.1 \cdot t_{SS}[ms] \quad (18)$$

C_{SS} is discharged by an internal 80-Ω FET when V_{OUT} is shutdown by EN, UVLO or thermal shutdown.

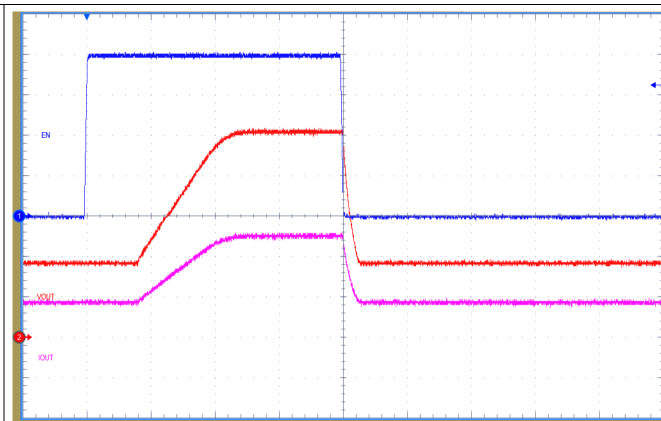
It is desirable in some applications for the output voltage to reach its nominal setpoint in the shortest possible time. Connecting a 100-kΩ resistor from SS to GND disables the LM5166's soft-start circuit, and the LM5166 operates in current limit during startup to rapidly charge the output capacitance.

Diode emulation mode (DEM) of the LM5166 prevents negative inductor current enabling monotonic startup under prebiased output conditions. With a prebiased output voltage, the LM5166 will wait until the soft-start ramp allows regulation above the prebiased voltage and then follow the soft-start ramp to the regulation setpoint as shown in Figure 44 and Figure 45.



Time Scale: 2 ms/Div CH2: V_{OUT}, 1 V/Div
CH1: V_{EN}, 1 V/Div CH4: I_{OUT}, 200 mA/Div

Figure 44. ENABLE On and Off; V_{OUT} Pre-biased to 1.8V Figure 50 Circuit, V_{IN} = 24 V, No Load



Time Scale: 2 ms/Div CH2: V_{OUT}, 1 V/Div
CH1: V_{EN}, 5 V/Div CH4: I_{OUT}, 200 mA/Div

Figure 45. ENABLE On and Off; V_{OUT} Pre-biased to 1.8V Figure 50 Circuit, V_{IN} = 24 V, 500 mA Load

7.3.9 Short-Circuit Operation

The LM5166 features a clamping circuit that clamps the SS pin about 175 mV above the FB pin (See Figure 46 and Figure 47). The circuit is enabled in COT mode and only works with the external soft-start capacitor.

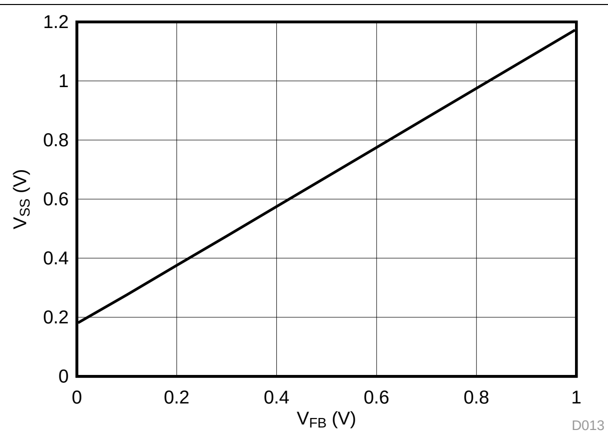


Figure 46. Soft-start Voltage vs Feedback Voltage

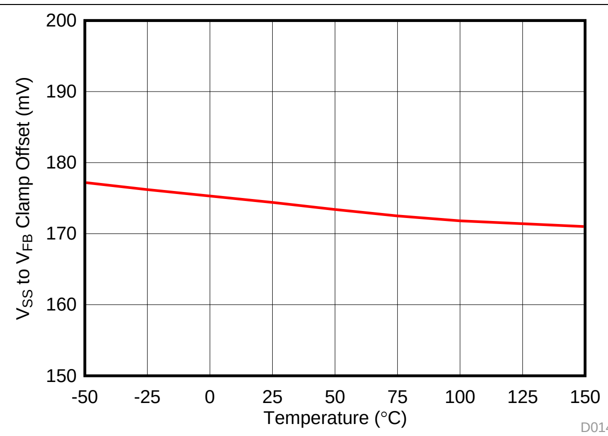
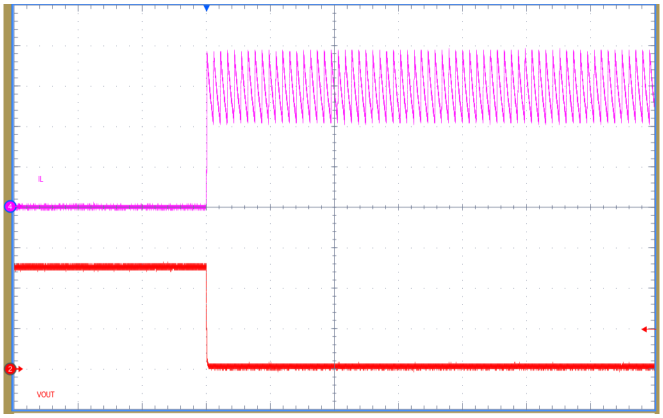


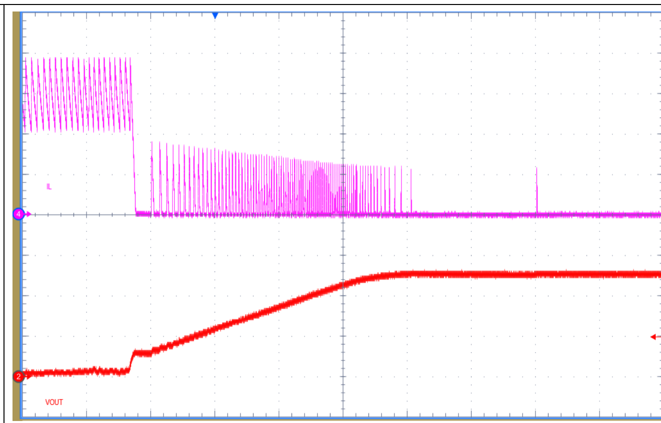
Figure 47. Soft-start to Feedback Clamp Offset vs Temperature

In case of an overload event such as an output short circuit, the clamping circuit discharges the soft-start capacitor. When the short is removed, the FB voltage quickly rises until it reaches the level of the SS pin. Then, the recovery continues under the soft-start capacitor control. Figure 48 and Figure 49 show short-circuit entry and recovery waveforms.



Time Scale: 1 ms/Div CH2: V_{OUT}, 2 V/Div CH4: I_L, 200 mA/Div

Figure 48. Short-Circuit Entry
Figure 50 Circuit



Time Scale: 1 ms/Div CH2: V_{OUT}, 2 V/Div CH4: I_L, 200 mA/Div

Figure 49. Short-Circuit Recovery
Figure 50 Circuit

7.3.10 Thermal Shutdown

Thermal shutdown is a built-in self protection to limit junction temperature and prevent damage related to over-heating. Thermal shutdown turns off the device when the junction temperature exceeds 170°C typically to prevent further power dissipation and temperature rise. Junction temperature decreases during thermal shutdown, and the LM5166 restarts when the junction temperature falls to 160°C.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides ON / OFF control for the LM5166. When V_{EN} is below 0.3 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 4 µA (typical) at V_{IN} = 12 V. The LM5166 also includes undervoltage protection of the internal bias LDO. If the internal bias supply voltage is below the UV threshold level, the switching regulator remains off.

7.4.2 Standby Mode

The internal bias LDO has a lower enable threshold than the switching regulator. When V_{EN} is above 0.6 V and below the precision enable threshold (1.22 V typically), the internal LDO is on and regulating. The precision enable circuitry is turned on if the LDO output is above the bias rail UV threshold. The switching action and output voltage regulation are disabled in the standby mode.

7.4.3 Active Mode – COT

The LM5166 is in active mode when V_{EN} is above the precision enable threshold and the internal bias rail is above its UV threshold level. In COT active mode, the LM5166 will operate in one of three modes depending on the load current:

1. CCM with fixed switching frequency when the load current is more than half of the peak-to-peak inductor current ripple;
2. Pulse skipping and diode emulation mode when load current is less than half of the peak-to-peak inductor current ripple of CCM operation;
3. Extended on-time mode when V_{IN} is nearly equal to V_{OUT} (dropout) and during load step transients.

7.4.4 Sleep Mode – COT

The LM5166 is in COT sleep mode when V_{EN} and V_{IN} are above their relevant threshold levels, FB has exceeded its upper hysteresis level, and the output capacitor is sourcing the load current. In COT sleep mode, the LM5166 operates with very low quiescent current (9.7 µA typical). There is a 2-µs wake-up delay from sleep to active modes.

7.4.5 Active Mode – PFM

The LM5166 is in PFM active mode when V_{EN} and V_{IN} are above their relevant thresholds, FB has fallen below the lower hysteresis level, and boundary conduction mode switching is recharging the output capacitor to the upper hysteresis level.

7.4.6 Sleep Mode – PFM

The LM5166 is in PFM sleep mode when V_{EN} and V_{IN} are above their relevant threshold levels, FB has exceeded the upper hysteresis level, and the output capacitor is sourcing the load current. In PFM sleep mode, the LM5166 operates with very low quiescent current (9.7 µA typical). There is a 2-µs wake-up delay from sleep to active modes.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5166 only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. To expedite and streamline the process of designing a LM5166-based converter, a comprehensive *LM5166 Quick-Start Design Tool* is available for download to assist the designer with component selection for a given application. WEBENCH® online software is also available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following sections discuss the design procedure for both COT and PFM modes using specific circuit design examples.

The LM5166 integrates several optional features to meet system design requirements, including precision enable, UVLO, programmable soft-start, programmable switching frequency in COT mode, adjustable current limit, and PGOOD indicator. Each application incorporates these features as needed for a more comprehensive design. The application circuits detailed below show LM5166 configuration options suitable for several application use cases. Please see the *LM5166EVM-C50A* and *LM5166EVM-C33A* EVM user's guides for more detail.

8.2 Typical Applications

8.2.1 Design 1: Wide V_{IN}, Low I_Q, High-Efficiency COT Converter Rated at 5 V, 500 mA

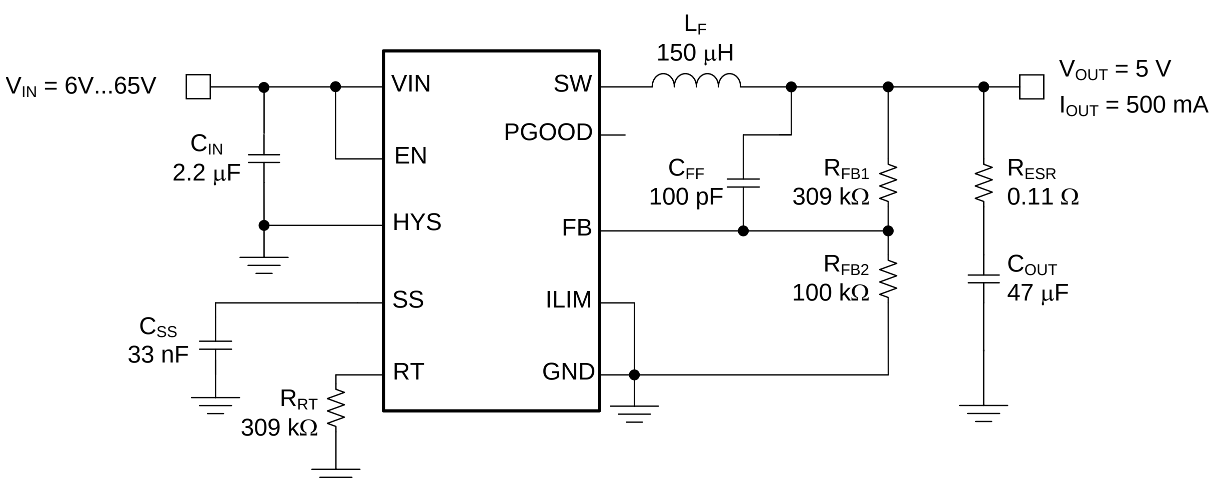


Figure 50. Schematic for Design 1 with $V_{IN(nom)}$ = 24 V, V_{OUT} = 5 V, $I_{OUT(max)}$ = 500 mA, $F_{SW(nom)}$ = 100 kHz

8.2.1.1 Design Requirements

The target efficiency is 90% for loads above 10 mA based on a nominal input voltage of 24 V and an output voltage of 5 V. The required input voltage range is 6 V to 65 V. The LM5166 is chosen to deliver a 5-V output voltage. The switching frequency is set at 100 kHz. The output voltage soft-start time is 4 ms. The required components are listed in Table 4.

Table 4. List of Components for Design 1[(1)]

Count	Ref Des	Description	Part Number	MFR
1	C_{IN}	Capacitor, Ceramic, 2.2 µF, 100 V, X7R, 10%, 1210	GRM32ER72A225KA35L	Murata
1	C_{OUT}	Capacitor, Ceramic, 47 µF, 10 V, X7R, 10%, 1210	GRM32ER71A476KE15L	Murata
1	C_{SS}	Capacitor, Ceramic, 0.033 µF, 10 V, X7R, 10%, 0402	Std	Std
1	C_{FF}	Capacitor, Ceramic, 100 pF, 50 V, X7R, 10%, 0402	Std	Std
1	L_F	Inductor, 150 µH, 0.240 Ω typ, 1.4 A Isat, 5 mm max	7447714151	Würth
		Inductor, 150 µH, 0.285 Ω typ, 1.12 A Isat, 5.1 mm max	CDRH105RNP-151NC	Sumida
1	R_{RT}	Resistor, Chip, 309 kΩ, 1/16W, 1%, 0402	Std	Std
1	R_{FB1}	Resistor, Chip, 309 kΩ, 1/16W, 1%, 0402	Std	Std
1	R_{ESR}	Resistor, Chip, 0.11 Ω, 1/16W, 1%, 0402	Std	Std
1	R_{FB2}	Resistor, Chip, 100 kΩ, 1/16W, 1%, 0402	Std	Std
1	U_1	IC, Synchronous Buck Converter, VSON-10, ADJ	LM5166QDRCRQ1	TI

(1) See Third-Party Products Disclaimer.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Feedback Resistors – R_{FB1}, R_{FB2}

The output voltage of the LM5166 is externally adjustable using a resistor divider network. The divider network comprises the upper feedback resistor R_{FB1} and lower feedback resistor R_{FB2} . Select R_{FB1} of 309 kΩ to minimize quiescent current and improve light-load efficiency in this application. With the desired output voltage setpoint of 5 V and V_{FB} = 1.223 V, calculate the resistance of R_{FB2} using Equation 15 to be 100.1 kΩ . Choose the closest available standard value of 100 kΩ for R_{FB2}. Please refer to Adjustable Output Voltage (FB) for more details.

8.2.1.2.2 Switching Frequency – R_T

The switching frequency of a COT-configured LM5166 is set by the on-time programming resistor at the RT pin. Using Equation 4, a standard 1% resistor of 309 kΩ gives a switching frequency of 92 kHz. Including the inductor R_{DCR} and R_{DSON1} in the calculation of t_{OFF} (Equation 3) gives us the adjusted F_{SW} of 101 kHz at 500 mA. The *LM5166 Quick-Start Design Tool* estimates and plots the switching frequency as a function of the load current.

Note that at very low duty cycles, the minimum controllable on-time of the high-side MOSFET, $T_{ON(min)}$, of 180 ns may affect choice of switching frequency. In CCM, $T_{ON(min)}$ limits the voltage conversion step-down ratio for a given switching frequency. The minimum controllable duty cycle is given by Equation 19.

$$D_{MIN} = T_{ON(min)} \cdot F_{SW} \tag{19}$$

Given a fixed $T_{ON(min)}$, it follows that higher switching frequency implies a larger minimum controllable duty cycle. Ultimately, the choice of switching frequency for a given output voltage affects the available input voltage range, solution size and efficiency. The maximum supply voltage for a given $T_{ON(min)}$ before switching frequency reduction occurs is given by Equation 20.

$$V_{IN(max)} = \frac{V_{OUT}}{T_{ON(min)} \cdot F_{SW}} \tag{20}$$

8.2.1.2.3 Filter Inductance – L_F

The inductor ripple current (assuming CCM operation) and peak inductor current are given respectively by Equation 21 and Equation 22.

$$\Delta I_L = \frac{V_{OUT}}{F_{SW} \cdot L_F} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{21}$$

$$I_{L(peak)} = I_{OUT(max)} + \frac{\Delta I_L}{2} \tag{22}$$

For most applications, choose the inductance such that the inductor ripple current, ΔI_L, is between 30% and 60% of the rated load current at nominal input voltage. Calculate the inductance using Equation 23.

$$L_F = \frac{V_{OUT}}{F_{SW} \cdot \Delta I_{L(nom)}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(nom)}}\right) \quad (23)$$

Choosing a 150-µH inductor in this design results in 295 mA peak-to-peak ripple current at nominal input voltage of 24 V, equivalent to 59% of the 500-mA rated load current. The peak inductor current at maximum input voltage of 65 V is 675 mA, which is sufficiently below the LM5166 peak current limit of 750 mA.

Check the inductor datasheet to ensure that the inductor saturation current is well above the current limit setting of a particular design. Ferrite designs have low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. However, ferrite core materials exhibit a hard saturation characteristic – the inductance collapses abruptly when the saturation current is exceeded. This results in an abrupt increase in inductor ripple current, higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that inductor saturation current generally decreases as the core temperature increases.

8.2.1.2.4 Output Capacitors – C_{OUT}

Select the output capacitor to limit the capacitive voltage ripple at the converter output. This is the sinusoidal ripple voltage that arises from the triangular ripple current flowing in the capacitor. Select an output capacitance using Equation 24 to limit the capacitive voltage ripple component to 0.5% of the output voltage.

$$C_{OUT} \geq \frac{\Delta I_{L(nom)}}{8 \cdot F_{SW} \cdot \Delta V_{OUT}} \quad (24)$$

Substituting $\Delta I_{L(nom)}$ of 295 mA and ΔV_{OUT} of 25 mV gives C_{OUT} greater than 16 µF. Mindful of the voltage coefficient of ceramic capacitors, select a 47-µF, 10-V capacitor with a high-quality dielectric.

8.2.1.2.5 Ripple Generation Network – R_{ESR}, C_{FF}

For this design, the Type 2 ripple generation method is selected as it offers a good balance between cost and output voltage ripple. For other methods refer to Ripple Generation Methods.

Select a series resistor, R_{ESR}, such that sufficient ripple in phase with the inductor current ripple appears at the feedback node, FB, using Equation 7 and Equation 8. Select a feed forward capacitor, C_{FF}, using Equation 9.

With $\Delta I_{L(nom)}$ of 295 mA at the nominal input voltage of 24 V, the required R_{ESR} is 0.11 Ω. Required feed-forward capacitance, C_{FF}, is 100 pF. Calculate the total output voltage ripple in CCM using Equation 25.

$$\Delta V_{OUT} = \Delta I_{L(nom)} \cdot \sqrt{R_{ESR}^2 + \left(\frac{1}{8 \cdot F_{SW} \cdot C_{OUT}}\right)^2} \quad (25)$$

8.2.1.2.6 Input Capacitor – C_{IN}

An input capacitor is necessary to limit the input ripple voltage while providing switching-frequency AC current to the buck power stage. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the VIN and GND pins of the LM5166. The input capacitors conduct a trapezoidal-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, the peak-to-peak input ripple voltage amplitude is given by Equation 26.

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1 - D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \quad (26)$$

The input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}, is given by Equation 27.

$$C_{IN} \geq \frac{I_{OUT} \cdot D \cdot (1 - D)}{F_{SW} \cdot (\Delta V_{IN} - I_{OUT} \cdot R_{ESR})} \quad (27)$$

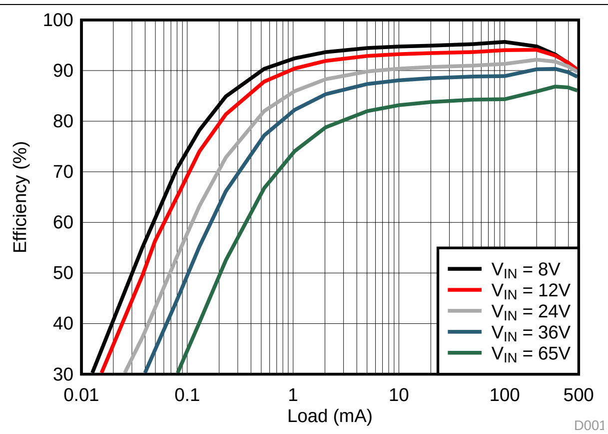
The recommended high-frequency input capacitance is 2.2 µF or higher and should be a high-quality ceramic with sufficient voltage rating. Based on the voltage coefficient of ceramic capacitors, choose a voltage rating of twice the maximum input voltage. Additionally, some bulk capacitance is required if the LM5166 circuit is not located within approximately 5 cm from the input voltage source. This capacitor provides damping to the resonance associated with parasitic inductance of the supply lines and high-Q ceramics.

8.2.1.2.7 Soft-start Capacitor – C_{SS}

Connect an external soft-start capacitor for a specific soft-start time. In this example, select a soft-start capacitance of 33 nF based on Equation 18 to achieve a soft-start time of 4 ms.

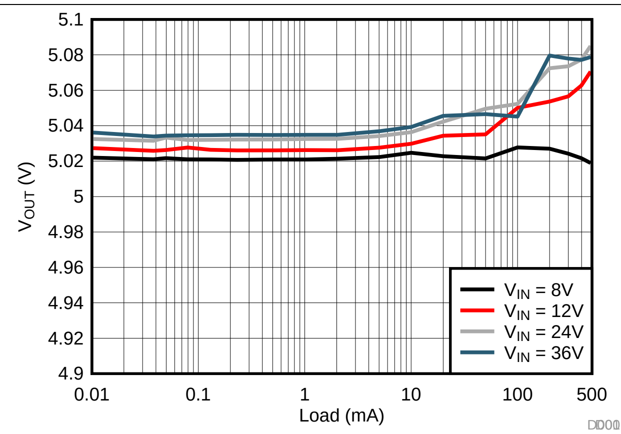
8.2.1.2.8 Application Performance Curves

Unless otherwise stated, application performance curves were taken at T_A = 25°C.



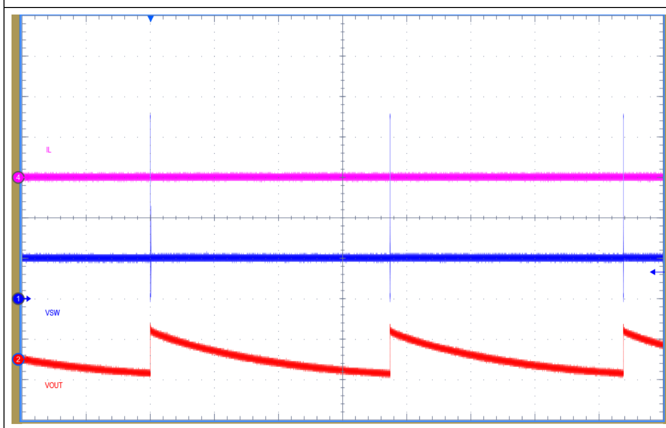
L_F = 150 µH
C_{OUT} = 47 µF
$F_{SW(nom)}$ = 100 kHz
R_{RT} = 309 kΩ

Figure 51. Converter Efficiency



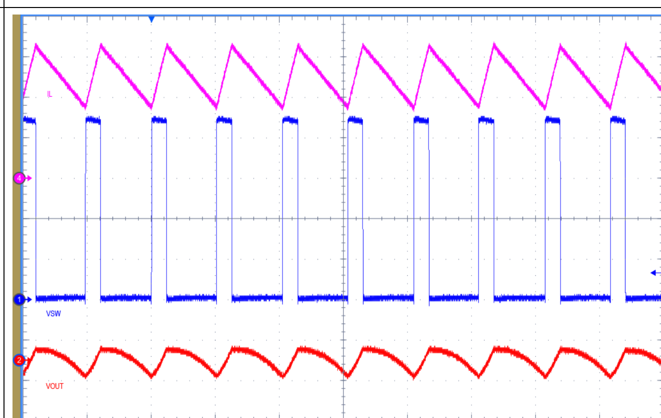
L_F = 150 µH
C_{OUT} = 47 µF
$F_{SW(nom)}$ = 100 kHz
R_{RT} = 309 kΩ

Figure 52. Converter Regulation



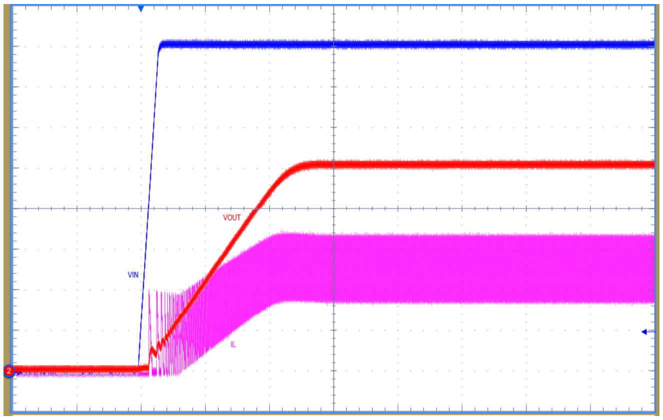
Time Scale: 20 ms/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 50 mV/Div
CH4: I_L, 200 mA/Div

Figure 53. No Load Switching Waveforms, V_{IN} = 24 V



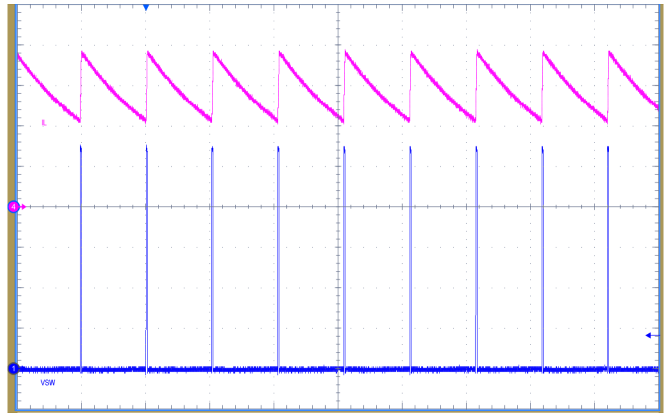
Time Scale: 10 µs/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 50 mV/Div
CH4: I_L, 200 mA/Div

Figure 54. Full Load Switching Waveforms, V_{IN} = 24 V



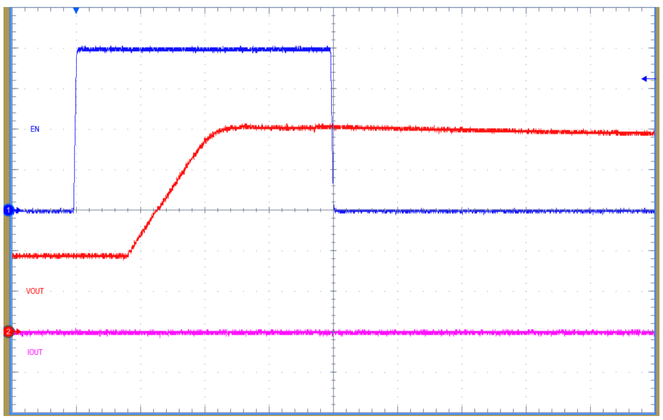
Time Scale: 2 ms/Div
CH1: V_{IN}, 3 V/Div
CH2: V_{OUT}, 1 V/Div
CH4: I_L, 200 mA/Div

Figure 55. Full Load Startup, V_{IN} = 24 V



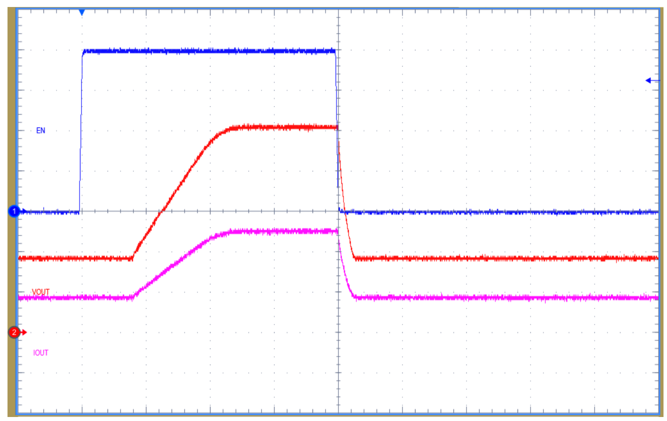
Time Scale: 100 µs/Div
CH1: V_{SW}, 4 V/Div
CH4: I_L, 200 mA/Div

Figure 56. Short Circuit, V_{IN} = 24 V



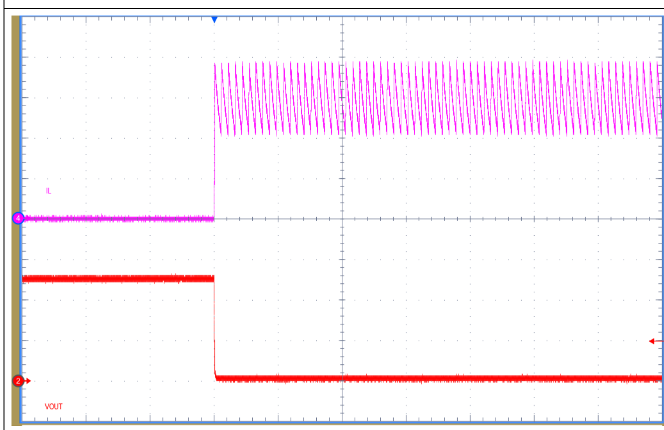
Time Scale: 2 ms/Div
CH1: V_{EN}, 1 V/Div
CH2: V_{OUT}, 1 V/Div
CH4: I_{OUT}, 200 mA/Div

Figure 57. ENABLE On and Off; V_{OUT} Pre-biased to 1.8V V_{IN} = 24 V, No Load



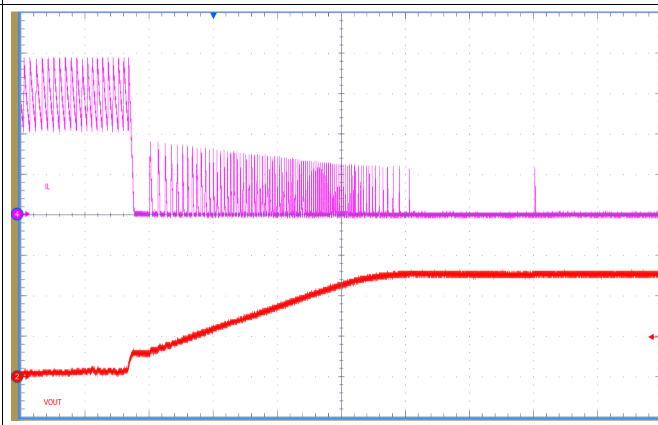
Time Scale: 2 ms/Div
CH1: V_{EN}, 5 V/Div
CH2: V_{OUT}, 1 V/Div
CH4: I_{OUT}, 200 mA/Div

Figure 58. ENABLE On and Off; V_{OUT} Pre-biased to 1.8V V_{IN} = 24 V, 500 mA Load



Time Scale: 1 ms/Div
CH2: V_{OUT}, 2 V/Div
CH4: I_L, 200 mA/Div

Figure 59. Short-Circuit Entry



Time Scale: 1 ms/Div
CH2: V_{OUT}, 2 V/Div
CH4: I_L, 200 mA/Div

Figure 60. Short-Circuit Recovery

8.2.2 Design 2: Wide V_{IN}, Low I_Q COT Converter Rated at 3.3 V, 500 mA

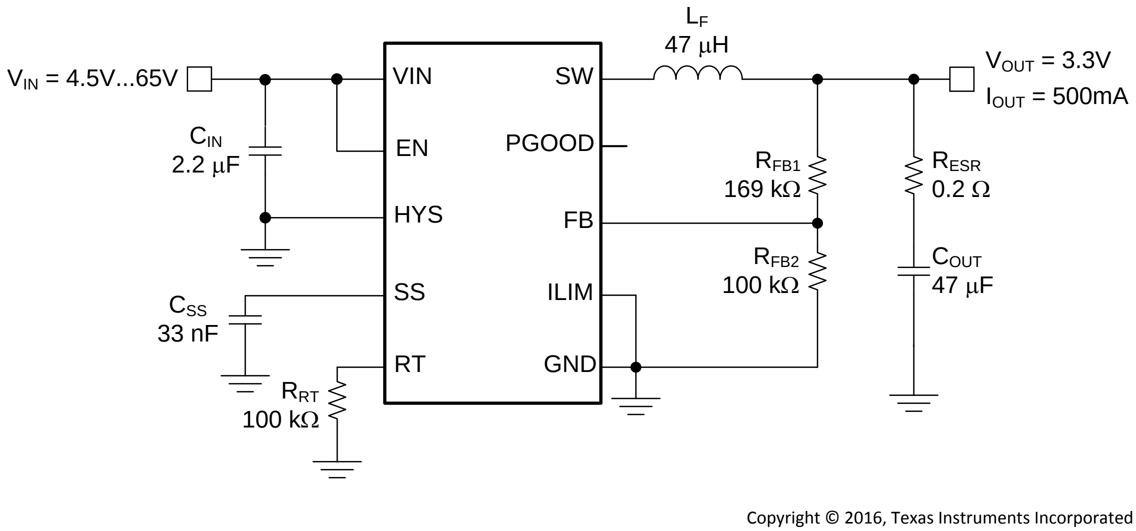


Figure 61. Schematic for Design 2 with $V_{IN(nom)}$ = 12 V, V_{OUT} = 3.3 V, $I_{OUT(max)}$ = 500 mA, $F_{SW(nom)}$ = 200 kHz

8.2.2.1 Design Requirements

The target efficiency is 85% for loads above 10 mA based on a nominal input voltage of 12 V and an output voltage of 3.3 V. The required input voltage range is 4.5 V to 65 V. The LM5166 is chosen to deliver a 3.3-V output voltage. The switching frequency is set at 200 kHz. The output voltage soft-start time is 4 ms. The required components are listed in Table 5.

Table 5. List of Components for Design 2[(1)]

Count	Ref Des	Description	Part Number	MFR
1	C_{IN}	Capacitor, Ceramic, 2.2 µF, 100 V, X7R, 10%, 1210	GRM32ER72A225KA35L	Murata
1	C_{OUT}	Capacitor, Ceramic, 47 µF, 10 V, X7R, 10%, 1210	GRM32ER71A476KE15L	Murata
1	C_{SS}	Capacitor, Ceramic, 0.033 µF, 10 V, X7R, 10%, 0402	Std	Std
1	L_F	Inductor, 47µH, 0.245Ω max, 1.2A Isat, 3.5mm max	LPS6235-473MR	Coilcraft
		Inductor, 47µH, 0.315Ω typ, 1.3A Isat, 2.8mm max	74404063470	Würth
1	R_{RT}	Resistor, Chip, 100 kΩ, 1/16W, 1%, 0402	Std	Std
1	R_{FB1}	Resistor, Chip, 169 kΩ, 1/16W, 1%, 0402	Std	Std
1	R_{ESR}	Resistor, Chip, 0.2 Ω, 1/16W, 1%, 0402	Std	Std
1	R_{FB2}	Resistor, Chip, 100 kΩ, 1/16W, 1%, 0402	Std	Std
1	U_1	IC, Synchronous Buck Converter, VSON-10, ADJ	LM5166QDRCRQ1	TI

(1) See Third-Party Products Disclaimer.

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Feedback Resistors – R_{FB1}, R_{FB2}

The output voltage of the LM5166 is externally adjustable using a resistor divider network. The divider network comprises the upper feedback resistor R_{FB1} and lower feedback resistor R_{FB2} . Select R_{FB1} of 169 kΩ to minimize quiescent current and improve light-load efficiency in this application. With the desired output voltage setpoint of 3.3 V and V_{FB} = 1.223 V, calculate the resistance of R_{FB2} using Equation 15 to be 100.1 kΩ . Choose the closest available standard value of 100 kΩ for R_{FB2}. Please refer to Adjustable Output Voltage (FB) for more detail.

8.2.2.2.2 Switching Frequency – R_T

The switching frequency of a COT-configured LM5166 is set by the on-time programming resistor at the RT pin. Using Equation 4, a standard 1% resistor of 100 kΩ gives a switching frequency of 190 kHz. Including the inductor R_{DCR} and R_{DSON1} in the calculation of t_{OFF} (Equation 3) gives us the adjusted F_{SW} of 215 kHz at 500 mA. The *LM5166 Quick-Start Design Tool* estimates and plots the switching frequency as a function of the load current.

Note that at very low duty cycles, the minimum controllable on-time of the high-side MOSFET, $T_{ON(min)}$, of 180 ns may affect choice of switching frequency. In CCM, $T_{ON(min)}$ limits the voltage conversion step-down ratio for a given switching frequency. The minimum controllable duty cycle is given by Equation 19.

Given a fixed $T_{ON(min)}$, it follows that higher switching frequency implies a larger minimum controllable duty cycle. Ultimately, the choice of switching frequency for a given output voltage affects the available input voltage range, solution size and efficiency. The maximum supply voltage for a given $T_{ON(min)}$ before switching frequency reduction occurs is given by Equation 20.

8.2.2.2.3 Filter Inductance – L_F

The inductor ripple current (assuming CCM operation) and peak inductor current are given respectively by Equation 21 and Equation 22.

For most applications, choose an inductance such that the inductor ripple current, ΔI_L, is between 30% and 60% of the rated load current at nominal input voltage. Calculate the inductance using Equation 23.

Choosing a 47-µH inductor in this design results in 275 mA peak-to-peak ripple current at nominal input voltage of 12 V, equivalent to 55% of the 500-mA rated load current. The peak inductor current at maximum input voltage of 65 V is 694 mA, which is sufficiently below the LM5166 peak current limit of 750 mA.

8.2.2.2.4 Output Capacitors – C_{OUT}

Select the output capacitor to limit the capacitive voltage ripple at the converter output. This is the sinusoidal ripple voltage that arises from the triangular ripple current flowing in the capacitor. Select an output capacitance using Equation 24 to limit the capacitive voltage ripple component to 0.5% of the output voltage.

Substituting $\Delta I_{L(nom)}$ of 275 mA and ΔV_{OUT} of 25 mV gives C_{OUT} greater than 11 µF. Mindful of the voltage coefficient of ceramic capacitors, select a 47-µF, 10-V capacitor with a high-quality dielectric.

8.2.2.2.5 Ripple Generation Network – R_{ESR}

For this design, the Type 1 ripple generation method is selected as it only requires a single external component. For other schemes refer to Ripple Generation Methods.

Select a series resistor, R_{ESR}, such that sufficient ripple in phase with the inductor current ripple appears at the feedback node, FB, using Equation 5 and Equation 6.

With $\Delta I_{L(nom)}$ of 275 mA at the nominal input voltage of 12 V, the required R_{ESR} is 0.2 Ω. Calculate the total output voltage ripple in CCM using Equation 25.

8.2.2.2.6 Input Capacitor – C_{IN}

An input capacitor is necessary to limit the input ripple voltage while providing switching-frequency AC current to the buck power stage. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the VIN and GND pins of the LM5166. The input capacitors conduct a trapezoidal-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, the peak-to-peak input ripple voltage amplitude is given by Equation 26.

The input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}, is given by Equation 27.

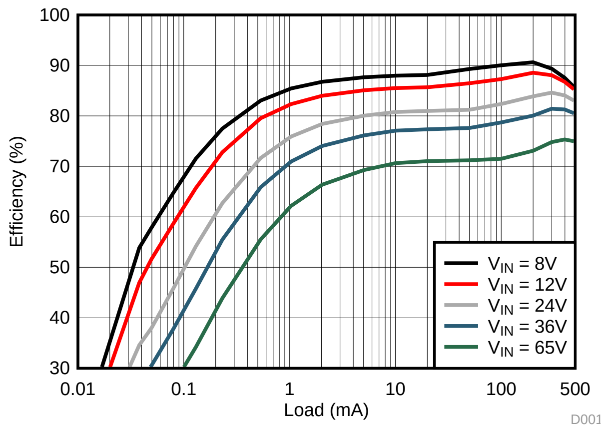
The recommended high-frequency capacitance is 2.2 μF or higher and should be a high-quality ceramic with sufficient voltage rating. Based on the voltage coefficient of ceramic capacitors, choose a voltage rating of twice the maximum input voltage. Additionally, some bulk capacitance is required if the LM5166 circuit is not located within approximately 5 cm from the input voltage source. This capacitor provides damping to the resonance associated with parasitic inductance of the supply lines and high-Q ceramics.

8.2.2.2.7 Soft-start Capacitor – C_{SS}

Connect an external soft-start capacitor for a specific soft-start time. In this example, select a soft-start capacitance of 33 nF based on Equation 18 to achieve a soft-start time of 4 ms.

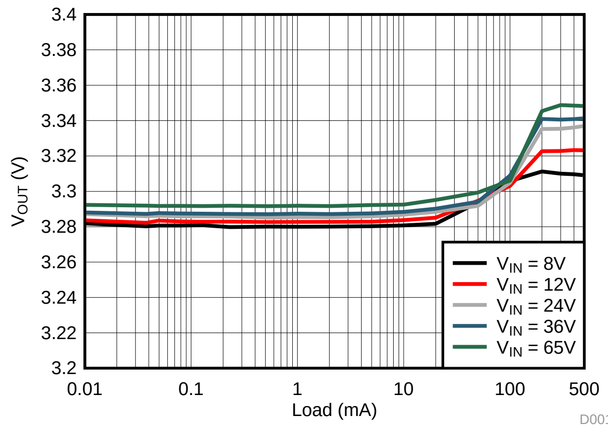
8.2.2.2.8 Application Performance Curves

Unless otherwise stated, application performance curves were taken at T_A = 25°C.



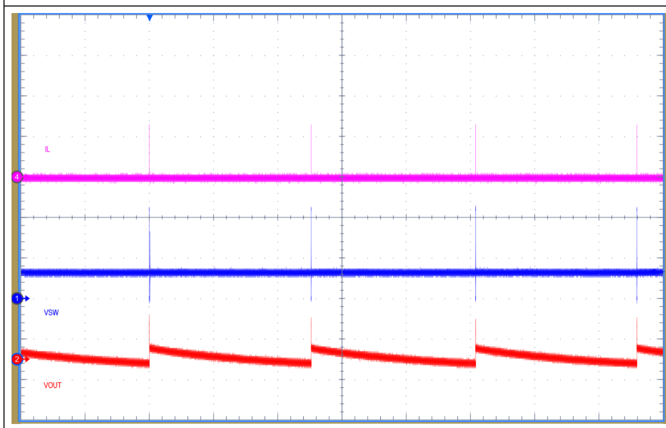
L_F = 47 µH
C_{OUT} = 47 µF
$F_{SW(nom)}$ = 200 kHz
R_{RT} = 100 kΩ

Figure 62. Converter Efficiency



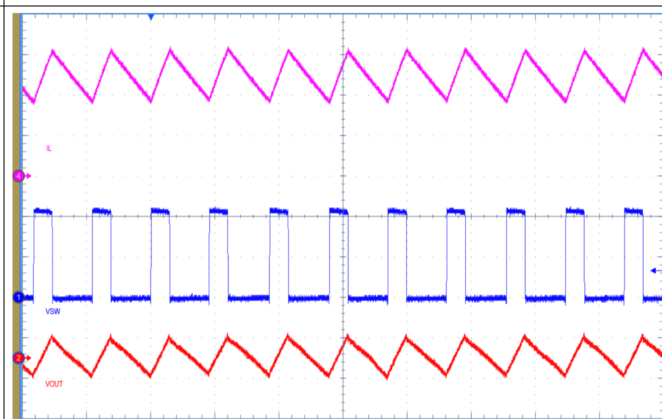
L_F = 47 µH
C_{OUT} = 47 µF
$F_{SW(nom)}$ = 200 kHz
R_{RT} = 100 kΩ

Figure 63. Converter Regulation



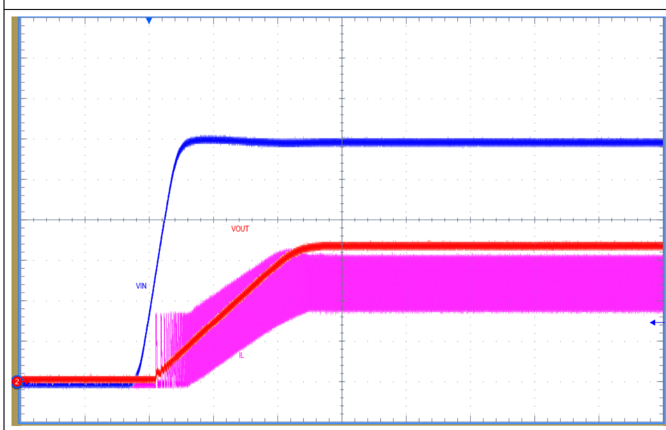
Time Scale: 20 ms/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 50 mV/Div
CH4: I_L, 200 mA/Div

Figure 64. No Load Switching Waveforms



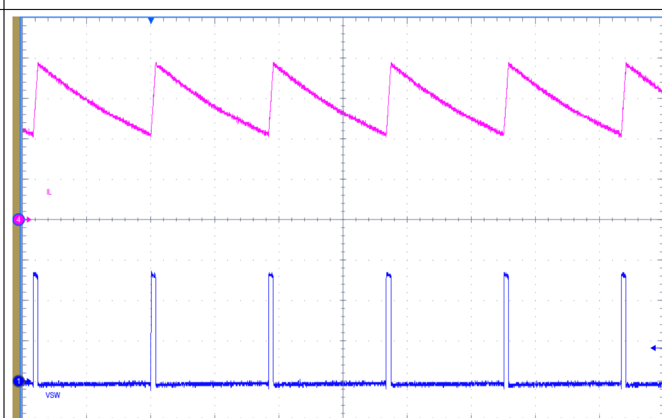
Time Scale: 5 µs/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 50 mV/Div
CH4: I_L, 200 mA/Div

Figure 65. Full Load Switching Waveforms



Time Scale: 2 ms/Div
CH1: V_{IN}, 2 V/Div
CH2: V_{OUT}, 1 V/Div
CH4: I_L, 200 mA/Div

Figure 66. Full Load Startup



Time Scale: 100 µs/Div
CH1: V_{SW}, 4 V/Div
CH4: I_L, 200 mA/Div

Figure 67. Short Circuit

8.2.3 Design 3: High-Density PFM Converter Rated at 3.3 V, 300 mA

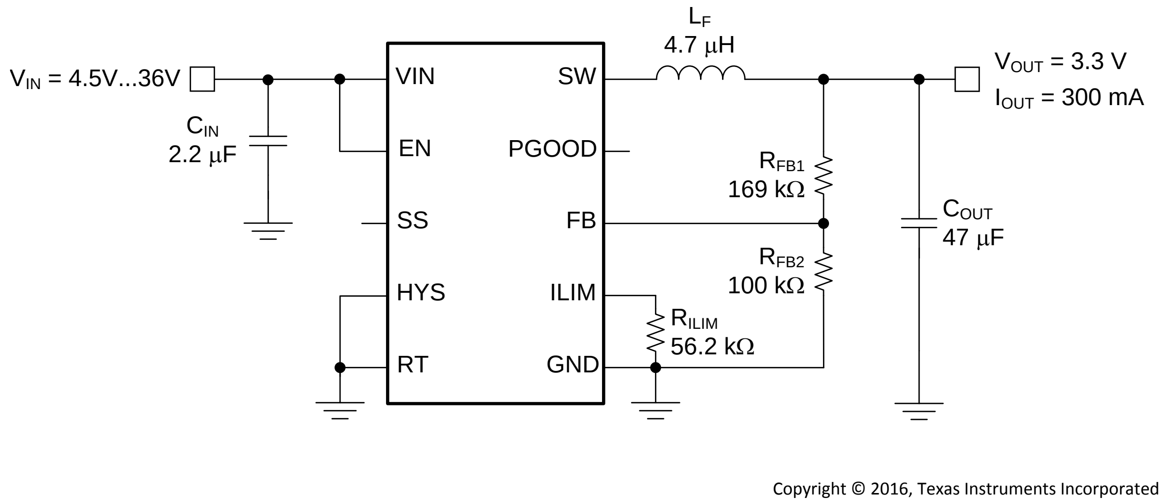


Figure 68. Schematic for Design 3 with $V_{IN(nom)}$ = 24 V, V_{OUT} = 3.3 V, $I_{OUT(max)}$ = 300 mA, $F_{SW(nom)}$ = 600 kHz

8.2.3.1 Design Requirements

The target efficiency is 75% for loads above 10 mA based on a nominal input voltage of 24 V, an output voltage of 3.3 V, with the emphasis on small solution size. The required input voltage range is 4.5 V to 36 V. The LM5166 has an internally-set soft-start time of 900 µs and an adjustable peak current limit threshold. The required components are listed in Table 6.

Table 6. List of Components for Design 3(1)

Count	Ref Des	Description	Part Number	MFR
1	C_{IN}	Capacitor, Ceramic, 2.2 µF, 50 V, X5R, 10%, 1206	GRM31CR71H225KA88	Murata
1	C_{OUT}	Capacitor, Ceramic, 47 µF, 6.3 V, X5R, 10%, 1206	GRM31CR60J476KE19	Murata
1	L_F	Inductor, 4.7 µH, 0.315 Ω typ, 2.2 A Isat, 1.2 mm max	TFM252012ALMA4R7TMAA	TDK
1	R_{ILIM}	Resistor, Chip, 56.2 kΩ, 1/16W, 1%, 0402	Std	Std
1	R_{FB1}	Resistor, Chip, 169 kΩ, 1/16W, 1%, 0402	Std	Std
1	R_{FB2}	Resistor, Chip, 100 kΩ, 1/16W, 1%, 0402	Std	Std
1	U_1	IC, Synchronous Buck Converter, VSON-10, ADJ	LM5166QDRCRQ1	TI

(1) See Third-Party Products Disclaimer.

8.2.3.2 Detailed Design Procedure

8.2.3.2.1 Feedback Resistors – R_{FB1}, R_{FB2}

The output voltage of the LM5166 is externally adjustable using a resistor divider network. The divider network comprises the upper feedback resistor R_{FB1} and lower feedback resistor R_{FB2}. Select R_{FB1} of 169 kΩ to minimize quiescent current and improve light-load efficiency in this application. With the desired output voltage setpoint of 3.3 V and V_{FB} = 1.223 V, calculate the resistance of R_{FB2} using Equation 15 as 99.5 kΩ. Choose the closest available standard value of 100 kΩ for R_{FB2}. Please refer to Adjustable Output Voltage (FB) for more detail.

8.2.3.2.2 Peak Current Limit Setting – R_{ILIM}

Install a 56.2 kΩ resistor from ILIM to GND to select a 750-mA peak current limit threshold setting to meet the rated output current of 300 mA. Please refer to Adjustable Current Limit for more detail.

8.2.3.2.3 Switching Frequency – L_F

Tie RT to GND to select PFM mode of operation. The inductor, input voltage, output voltage and peak current determine the pulse switching frequency of a PFM-configured LM5166. For a given input voltage, output voltage and peak current, the inductance of L_F sets the switching frequency when the output is in regulation. Use Equation 28 to select an inductance of 4.7 µH based on the target PFM converter switching frequency of 600 kHz at 24-V input.

$$L_F = \frac{V_{OUT}}{F_{SW(PFM)} \cdot I_{PK(PFM)}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{28}$$

$I_{PK(PFM)}$ in this example is the peak current limit setting of 750 mA plus the inductor current overshoot resulting from the 80-ns peak current comparator delay, t_{ILIM_delay}. An additional constraint on the inductance is the 180-ns minimum on-time of the high-side MOSFET. Therefore, in order to keep the inductor current well controlled, choose an inductance that is larger than $L_{F(min)}$ using Equation 29 where $V_{IN(max)}$ is the maximum input supply voltage for the application, t_{ILIM_delay} is 80 ns, $t_{ON(min)}$ is 180 ns, the maximum current limit threshold, $I_{LIM(max)}$, is 825 mA, and the maximum allowed peak inductor current, $I_{L(max)}$, is 1.6 A.

$$L_{F(min)} = \mathrm{Max}\left(\frac{V_{IN(max)} \cdot t_{ON(min)}}{I_{L(max)}}, \frac{V_{IN(max)} \cdot t_{ILIM\_delay}}{I_{L(max)} - I_{LIM(max)}}\right) \tag{29}$$

Choose an inductor with saturation current rating above the peak current limit setting, and allow for derating of the saturation current at the highest expected operating temperature.

8.2.3.2.4 Output Capacitors – C_{OUT}

The output capacitor, C_{OUT}, filters the inductor's ripple current and stores energy to meet the load current requirement when the LM5166 is in sleep mode. The output ripple has a base component of amplitude V_{OUT} /123 related to the typical feedback comparator hysteresis in PFM. The wakeup time from sleep to active mode adds a ripple voltage component that is a function of the output current. Approximate the total output ripple by Equation 30.

$$\Delta V_{OUT} = \left(\frac{I_{PK(PFM)}}{2} + I_{OUT}\right) \cdot \frac{1\mu s}{C_{OUT}} + \frac{V_{OUT}}{123} \tag{30}$$

Also, the output capacitance must be large enough to accept the energy stored in the inductor without a large deviation in output voltage. Setting this voltage change equal to 1% of the output voltage results in a C_{OUT} requirement defined with Equation 31.

$$C_{OUT} \geq 50 \cdot L_F \cdot \left(\frac{I_{PK(PFM)}}{V_{OUT}}\right)^2 \tag{31}$$

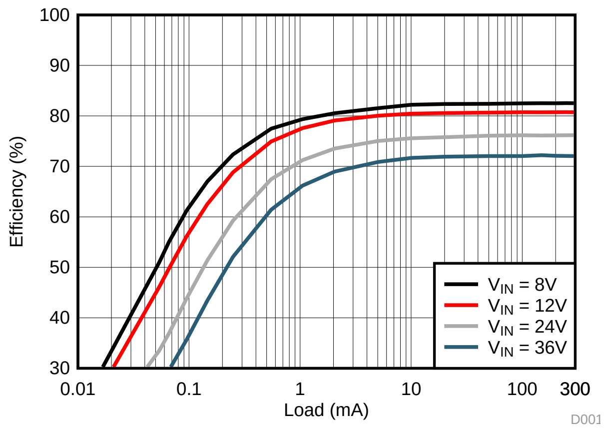
In general, select the capacitance of C_{OUT} to limit the output voltage ripple at full load current, ensuring that it is rated for worst-case RMS ripple current given by $I_{RMS} = I_{PK(PFM)}$ /2. In this design example, select a 47-µF, 6.3-V capacitor with a high-quality dielectric.

8.2.3.2.5 Input Capacitor – C_{IN}

The input capacitor, C_{IN}, filters the high-side MOSFET's triangular current waveform, see Figure 82. To prevent large ripple voltage, use a low ESR ceramic input capacitor sized for the worst-case RMS ripple current given by $I_{RMS} = I_{OUT}$ /2. In this design example, choose a 2.2-µF, 50-V ceramic input capacitor with a high-quality dielectric.

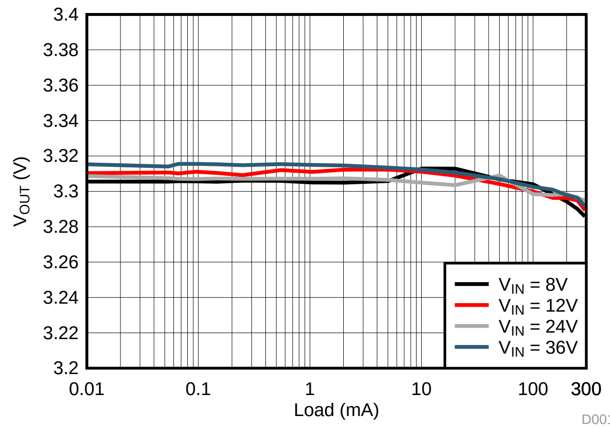
8.2.3.2.6 Application Performance Curves

Unless otherwise stated, application performance curves were taken at T_A = 25°C.



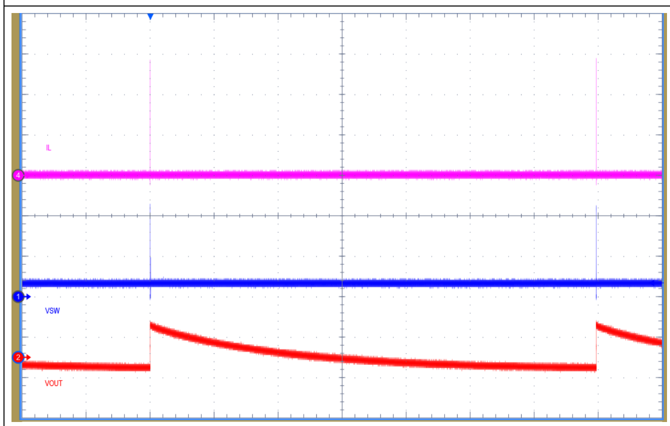
L_F = 4.7 µH
C_{OUT} = 47 µF
$F_{SW(nom)}$ = 600 kHz
R_{RT} = 0 Ω

Figure 69. Converter Efficiency



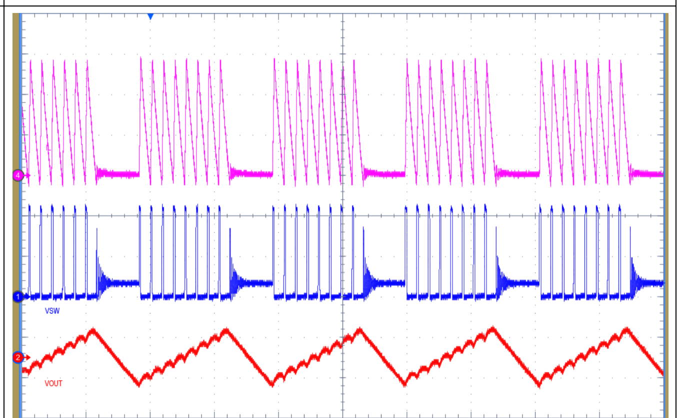
L_F = 4.7 µH
C_{OUT} = 47 µF
$F_{SW(nom)}$ = 600 kHz
R_{RT} = 0 Ω

Figure 70. Converter Regulation



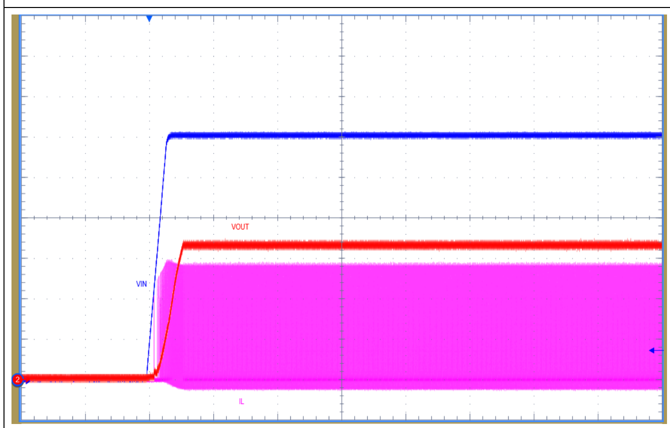
Time Scale: 20 ms/Div
CH1: V_{SW}, 10 V/Div
CH2: V_{OUT}, 50 mV/Div
CH4: I_L, 400 mA/Div

Figure 71. No Load Switching Waveforms, V_{IN} = 24 V



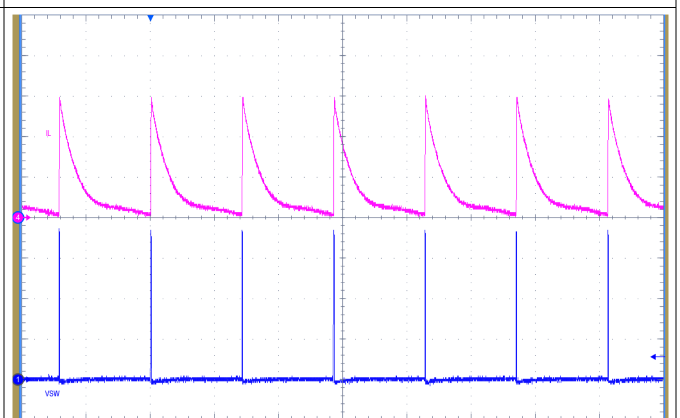
Time Scale: 10 µs/Div
CH1: V_{SW}, 10 V/Div
CH2: V_{OUT}, 50 mV/Div
CH4: I_L, 400 mA/Div

Figure 72. Full Load Switching Waveforms, V_{IN} = 24 V



Time Scale: 2 ms/Div
CH1: V_{IN}, 4 V/Div
CH2: V_{OUT}, 1 V/Div
CH4: I_L, 400 mA/Div

Figure 73. Full Load Startup, V_{IN} = 24 V



Time Scale: 20 µs/Div
CH1: V_{SW}, 6 V/Div
CH4: I_L, 400 mA/Div

Figure 74. Short Circuit, V_{IN} = 24 V

8.2.4 Design 4: Wide V_{IN}, Low I_Q PFM Converter Rated at 5 V, 500 mA

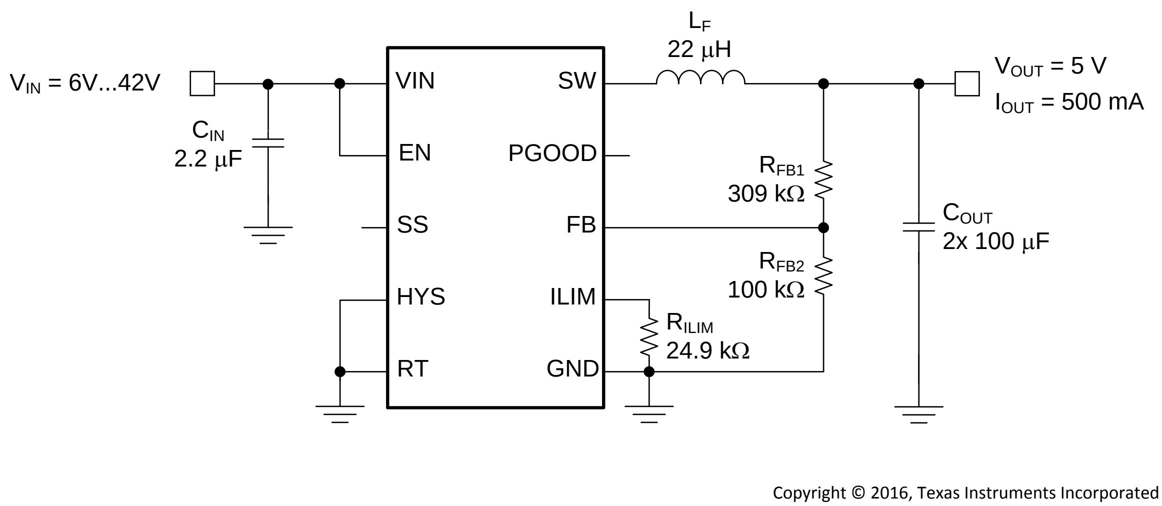


Figure 75. Schematic for Design 4 with $V_{IN(nom)}$ = 12 V, V_{OUT} = 5 V, $I_{OUT(max)}$ = 500 mA, $F_{SW(nom)}$ = 100 kHz

8.2.4.1 Design Requirements

The target efficiency is 85% for loads above 1 mA based on a nominal input voltage of 12 V, an output voltage of 5 V. The required input voltage range is 6 V to 42 V. The LM5166 has an internally-set soft-start time of 900 µs and an adjustable peak current limit threshold. The required components are listed in Table 7.

Table 7. List of Components for Design 4[1]

Count	Ref Des	Description	Part Number	MFR
1	C_{IN}	Capacitor, Ceramic, 2.2 µF, 50 V, X7R, 10%, 1206	GRM31CR71H225KA88L	Murata
2	C_{OUT}	Capacitor, Ceramic, 100 µF, 10 V, X5R, 10%, 1210	GRM32ER61A107ME20K	Murata
1	L_F	Inductor, 22µH, 0.145Ω max, 1.7A Isat, 3.5mm max	LPS6235-223MR	Coilcraft
1	R_{ILIM}	Resistor, Chip, 24.9 kΩ, 1/16W, 1%, 0402	Std	Std
1	R_{FB1}	Resistor, Chip, 309 kΩ, 1/16W, 1%, 0402	Std	Std
1	R_{FB2}	Resistor, Chip, 100 kΩ, 1/16W, 1%, 0402	Std	Std
1	U_1	IC, Synchronous Buck Converter, VSON-10, ADJ	LM5166QDRCRQ1	TI

(1) See Third-Party Products Disclaimer.

8.2.4.2 Detailed Design Procedure

8.2.4.2.1 Feedback Resistors – R_{FB1}, R_{FB2}

The output voltage of the LM5166 is externally adjustable using a resistor divider network. The divider network comprises the upper feedback resistor R_{FB1} and lower feedback resistor R_{FB2}. Select R_{FB1} of 309 kΩ to minimize quiescent current and improve light-load efficiency in this application. With the desired output voltage setpoint of 5 V and V_{FB} = 1.223 V, calculate the resistance of R_{FB2} using Equation 15 as 99.5 kΩ. Choose the closest available standard value of 100 kΩ for R_{FB2}. Please refer to Adjustable Output Voltage (FB) for more detail.

8.2.4.2.2 Peak Current Limit Setting – R_{ILIM}

Install a 24.9 kΩ resistor from ILIM to GND to select a 1.25-A peak current limit threshold setting with modulated ILIM function to meet the rated output current of 500 mA and the efficiency target. Please refer to Adjustable Current Limit for more detail.

8.2.4.2.3 Switching Frequency – L_F

Tie RT to GND to select PFM mode of operation. The inductor, input voltage, output voltage and peak current determine the pulse switching frequency of a PFM-configured LM5166. For a given input voltage, output voltage and peak current, the inductance of L_F sets the switching frequency when the output is in regulation. Use Equation 28 to select an inductance of 22 µH based on the target PFM converter switching frequency of 100 kHz at 12-V input.

$I_{PK(PFM)}$ in this example is the peak current limit setting of 1.25 A plus the inductor current overshoot resulting from the 80-ns peak current comparator delay. An additional constraint on the inductance is the 180-ns minimum on-time of the high-side MOSFET. Therefore, in order to keep the inductor current well controlled, choose an inductance that is larger than $L_{F(min)}$ using Equation 29.

Choose an inductor with saturation current rating above the peak current limit setting, and allow for derating of the saturation current at the highest expected operating temperature.

8.2.4.2.4 Output Capacitors – C_{OUT}

The output capacitor, C_{OUT}, filters the inductor's ripple current and stores energy to meet the load current requirement when the LM5166 is in sleep mode. The output ripple has a base component of amplitude V_{OUT} /123 related to the typical feedback comparator hysteresis in PFM. The wakeup time from sleep to active mode adds a ripple voltage component that is a function of the output current. Approximate the total output ripple by Equation 30.

Also, the output capacitance must be large enough to accept the energy stored in the inductor without a large deviation in output voltage. Setting this voltage change equal to 1% of the output voltage results in a C_{OUT} requirement defined with Equation 31.

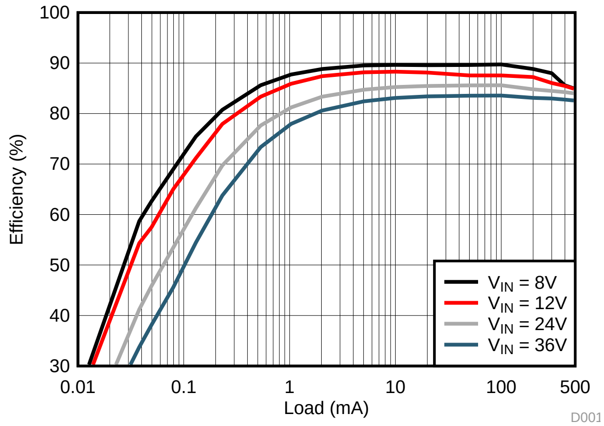
In general, select the capacitance of C_{OUT} to limit the output voltage ripple at full load current, ensuring that it is rated for worst-case RMS ripple current given by $I_{RMS} = I_{PK(PFM)}$ /2. In this design example, select two 100-µF, 10-V capacitors with a high-quality dielectric.

8.2.4.2.5 Input Capacitor – C_{IN}

The input capacitor, C_{IN}, filters the high-side MOSFET's triangular current waveform, see Figure 82. To prevent large ripple voltage, use a low ESR ceramic input capacitor sized for the worst-case RMS ripple current given by $I_{RMS} = I_{OUT}$ /2. In this design example, choose a 2.2-µF, 50-V ceramic input capacitor with a high-quality dielectric.

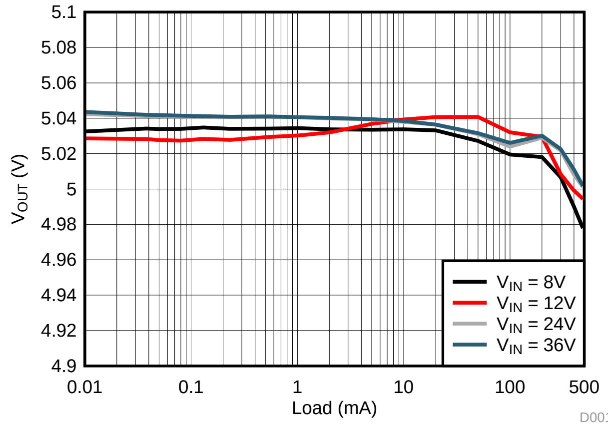
8.2.4.3 Application Performance Curves

Unless otherwise stated, application performance curves were taken at T_A = 25°C.



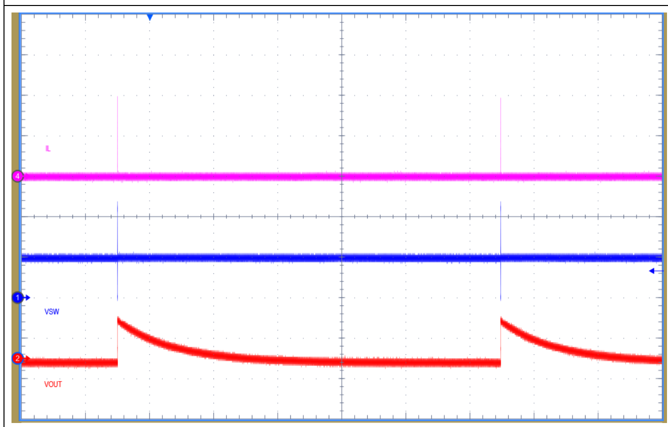
L_F = 22 µH　　$F_{SW(nom)}$ = 100 kHz
C_{OUT} = 200 µF　　R_{RT} = 0 Ω

Figure 76. Converter Efficiency



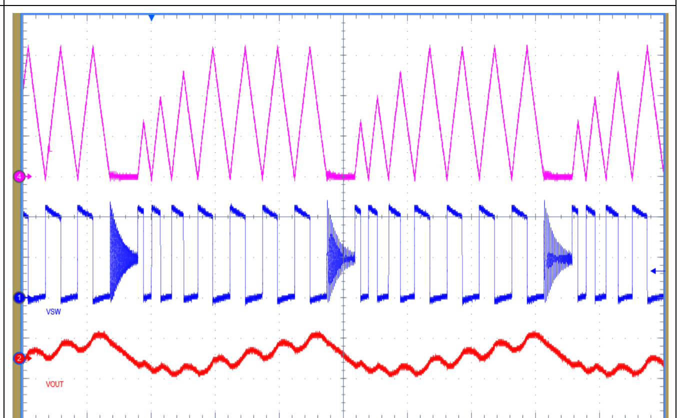
L_F = 22 µH　　$F_{SW(nom)}$ = 100 kHz
C_{OUT} = 200 µF　　R_{RT} = 0 Ω

Figure 77. Converter Regulation



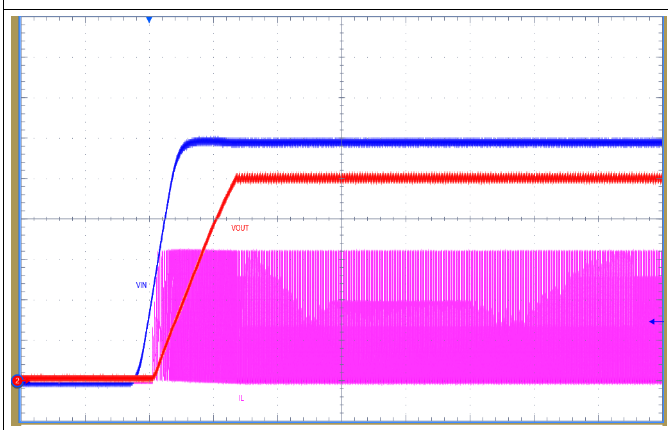
Time Scale: 50 ms/Div　　CH2: V_{OUT}, 50 mV/Div
CH1: V_{SW}, 5 V/Div　　CH4: I_L, 400 mA/Div

Figure 78. No Load Switching Waveforms



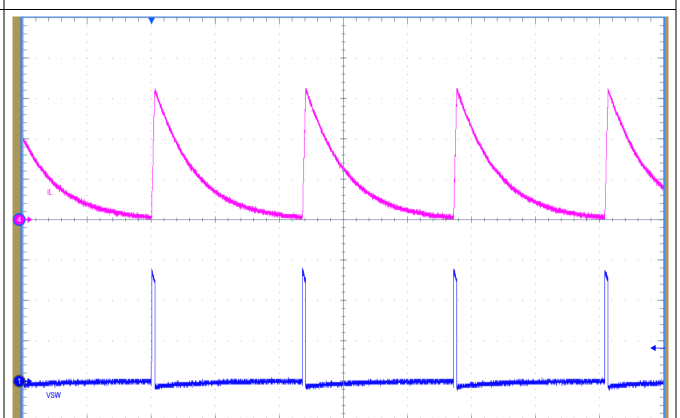
Time Scale: 20 µs/Div　　CH2: V_{OUT}, 100 mV/Div
CH1: V_{SW}, 5 V/Div　　CH4: I_L, 400 mA/Div

Figure 79. Full Load Switching Waveforms



Time Scale: 2 ms/Div　　CH2: V_{OUT}, 1 V/Div
CH1: V_{IN}, 2 V/Div　　CH4: I_L, 400 mA/Div

Figure 80. Full Load Startup



Time Scale: 50 µs/Div　　CH4: I_L, 400 mA/Div
CH1: V_{SW}, 4 V/Div

Figure 81. Short Circuit

9 Power Supply Recommendations

The LM5166 is designed to operate from an input voltage supply range between 3 V and 65 V. This input supply should be able to withstand the maximum input current and maintain a voltage above 3 V. Ensure that the resistance of the input supply rail is low enough that an input current transient does not cause a high enough drop at the LM5166 supply voltage to cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LM5166 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A 10-µF electrolytic capacitor is a typical choice for this function, whereby the capacitor ESR provides a level of damping against input filter resonances. A typical ESR of 0.5 Ω provides enough damping for most input circuit configurations.

10 PCB Layout

The performance of any switching converter depends as much upon PCB layout as it does the component selection. The following guidelines are provided to assist with designing a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

10.1 PCB Layout Guidelines

PCB layout is a critical portion of good power supply design. There are several paths that conduct high slew-rate currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise and EMI or degrade the power supply performance.

1. To help eliminate these problems, bypass the VIN pin to GND with a low ESR ceramic bypass capacitor with a high-quality dielectric. Place C_{IN} as close as possible to the LM5166 VIN and GND pins. Grounding for both the input and output capacitors should consist of localized top-side planes that connect to the GND pin and GND PAD.
2. Minimize the loop area formed by the input filter capacitor connections to the VIN and GND pins.
3. Locate the filter inductor close to the SW pin. Minimize the area of the SW trace/plane to prevent excessive capacitive coupling.
4. Tie the GND pin directly to the power pad under the device and to a heat-sinking PCB ground plane.
5. Use a ground plane in one of the middle layers as noise shielding and heat dissipation path.
6. Have a single-point ground connection to the plane. Route the ground connections for the feedback, soft-start, and enable components to the ground plane. This prevents any switched or load currents from flowing in analog ground traces. If not properly handled, poor grounding results in degraded load regulation or erratic output voltage ripple behavior.
7. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
8. Minimize trace length to the FB pin. Locate both feedback resistors, R_{FB1} and R_{FB2} close to the FB pin. Place C_{FF} (if needed) directly in parallel with R_{FB1}. If output setpoint accuracy at the load is important, connect the V_{OUT} sense at the load. Route the V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielding layer.
9. The RT pin is sensitive to noise. Thus, locate the R_{RT} resistors as close as possible to the device and route with minimal lengths of trace. The parasitic capacitance from RT to GND must not exceed 20 pF.
10. Provide adequate heat-sinking for the LM5166 to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pad to the PCB ground plane. If the PCB has multiple copper layers, these thermal vias should also be connected to inner layer heat-spreading ground planes.

10.1.1 Compact PCB Layout for EMI Reduction

Radiated EMI generated by high di/dt components relates to pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimize radiated EMI is to identify the pulsing current path and minimize the area of that path.

The critical switching loop of the power stage in terms of EMI is denoted in Figure 82. The topological architecture of a buck converter means that a particularly high di/dt current path exists in the loop comprising the input capacitor and the LM5166's integrated MOSFETs, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing the effective loop area.

PCB Layout Guidelines (continued)

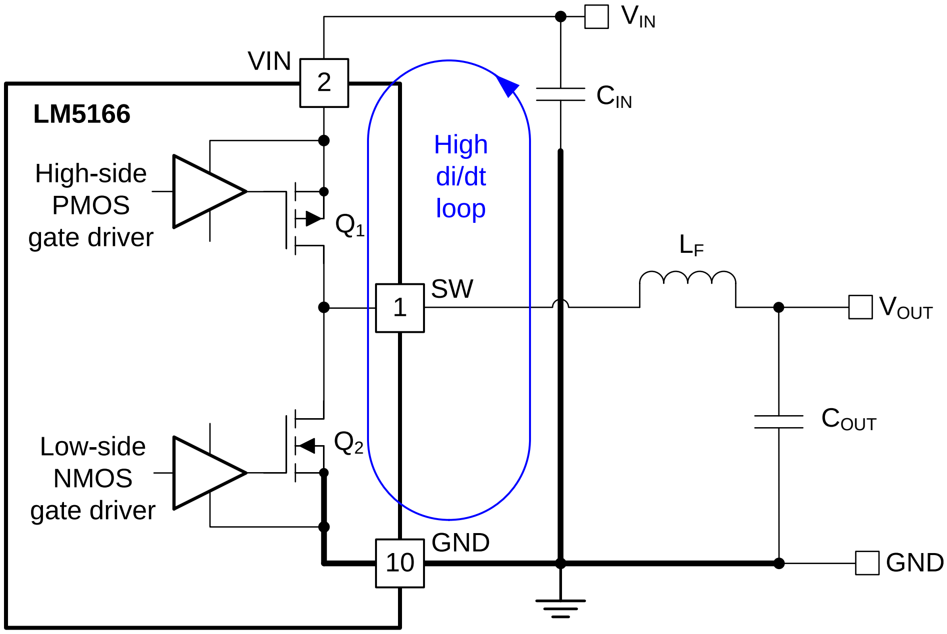


Figure 82. DC/DC Buck Regulator with Power Stage Circuit Switching Loops

The input capacitor provides the primary path for the high di/dt components of the high-side MOSFET's current. Placing a ceramic capacitor as close as possible to the VIN and GND pins is the key to EMI reduction. Keep the trace connecting SW to the inductor as short as possible and just wide enough to carry the load current without excessive heating. Use short, thick traces or copper pours (shapes) for current conduction path to minimize parasitic resistance. Place the output capacitor close to the V_{OUT} side of the inductor, and connect the capacitor's return terminal to the LM5166's GND pin and exposed PAD.

10.1.2 Feedback Resistors

For the adjustable output voltage version of the LM5166, reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. This reduces the trace length of FB signal and noise coupling. This reduces the trace length of FB signal and noise coupling. The FB pin is the input to the feedback comparator, and as such is a high impedance node sensitive to noise. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if a short path is not available.

Route the voltage sense trace from the load to the feedback resistor divider, keeping away from the SW node, the inductor and V_{IN} to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high feedback resistances, greater than 100 kΩ, are used to set the output voltage. Also, route the voltage sense trace on a different layer from the inductor, SW node and V_{IN}, such that there is a ground plane that separates the feedback trace from the inductor and SW node copper polygon. This provides further shielding for the voltage feedback path from switching noise sources

10.2 Layout Example

Figure 83 shows an example layout for the PCB top layer of a 4-layer board with essential components located on the top side. The bottom layer features optional Type 3 ripple generation components (R_A and C_A), and R_{UV1}, R_{UV2}, and R_{HYS} resistors.

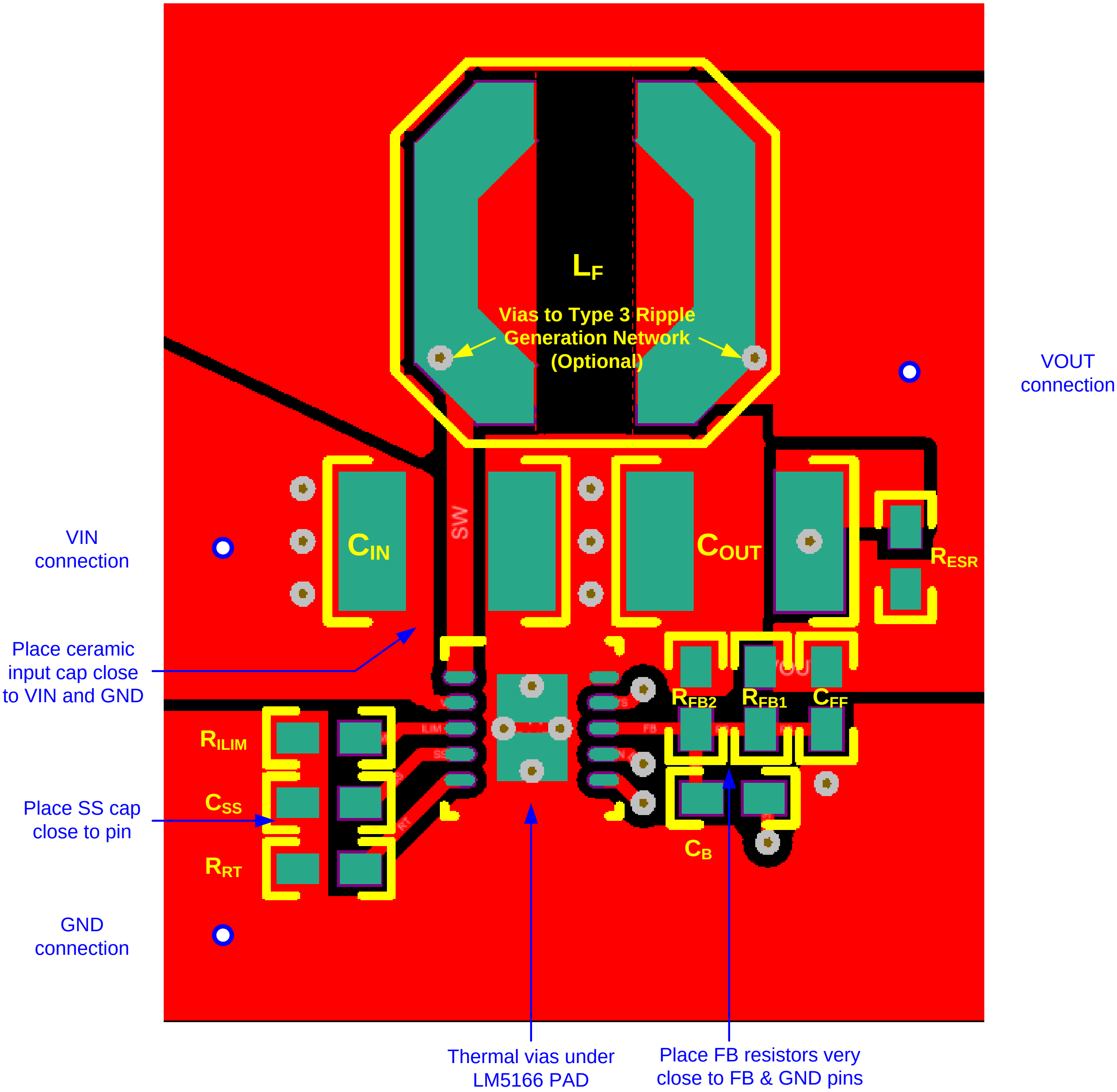


Figure 83. LM5166 Single-Sided PCB Layout Example

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

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11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Development Support

- LM5166 *Quick-Start Design Tool*
- LM5166 *Simulation Models*
- For TI's Reference Design Library, visit TIDesigns
- For TI's WEBENCH Design Environment, visit the WEBENCH® Design Center

11.4 Documentation Support

- *LM5166EVM-C50A User's Guide*, SNVU485
- *LM5166EVM-C33A User's Guide*, SNVU544
- TI Designs:
  - TIDA-01358 Design Reference Guide: *24Vac Power Stage with USB Capability Reference Design for Smart Thermostat or Gateway*, TIDUCE1
- *AN-2162: Simple Success with Conducted EMI from DC-DC Converters*, SNVA489
- *Automotive Cranking Simulator User's Guide*, SLVU984
- *Using New Thermal Metrics Application Report*, SBVA025
- *Semiconductor and IC Package Thermal Metrics*, SPRA953

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5166DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	5166	Samples
LM5166DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	5166	Samples
LM5166XDRCR	PREVIEW	VSON	DRC	10	3000	TBD	Call TI	Call TI	-40 to 150		
LM5166XDRCT	PREVIEW	VSON	DRC	10	250	TBD	Call TI	Call TI	-40 to 150		
LM5166YDRCR	PREVIEW	VSON	DRC	10	3000	TBD	Call TI	Call TI	-40 to 150		
LM5166YDRCT	PREVIEW	VSON	DRC	10	250	TBD	Call TI	Call TI	-40 to 150		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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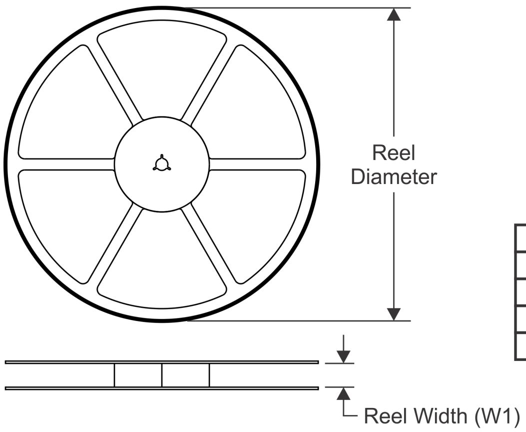
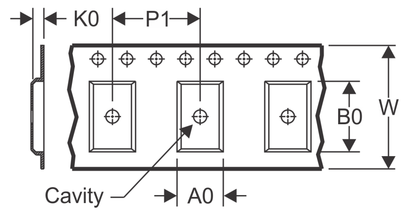
TAPE AND REEL INFORMATION

REEL DIMENSIONS

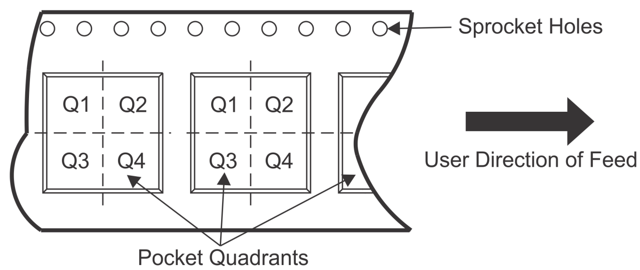


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

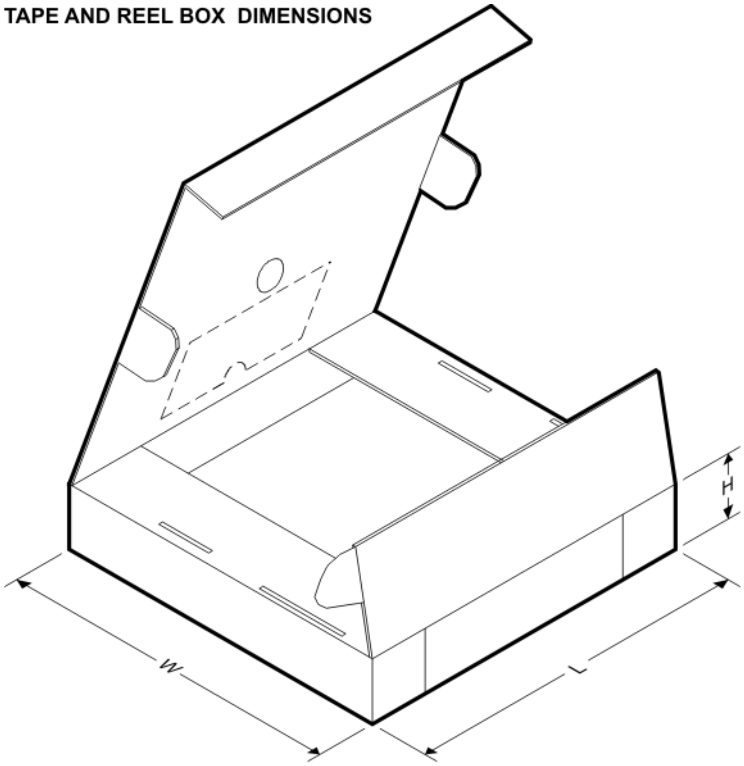
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5166DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM5166DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

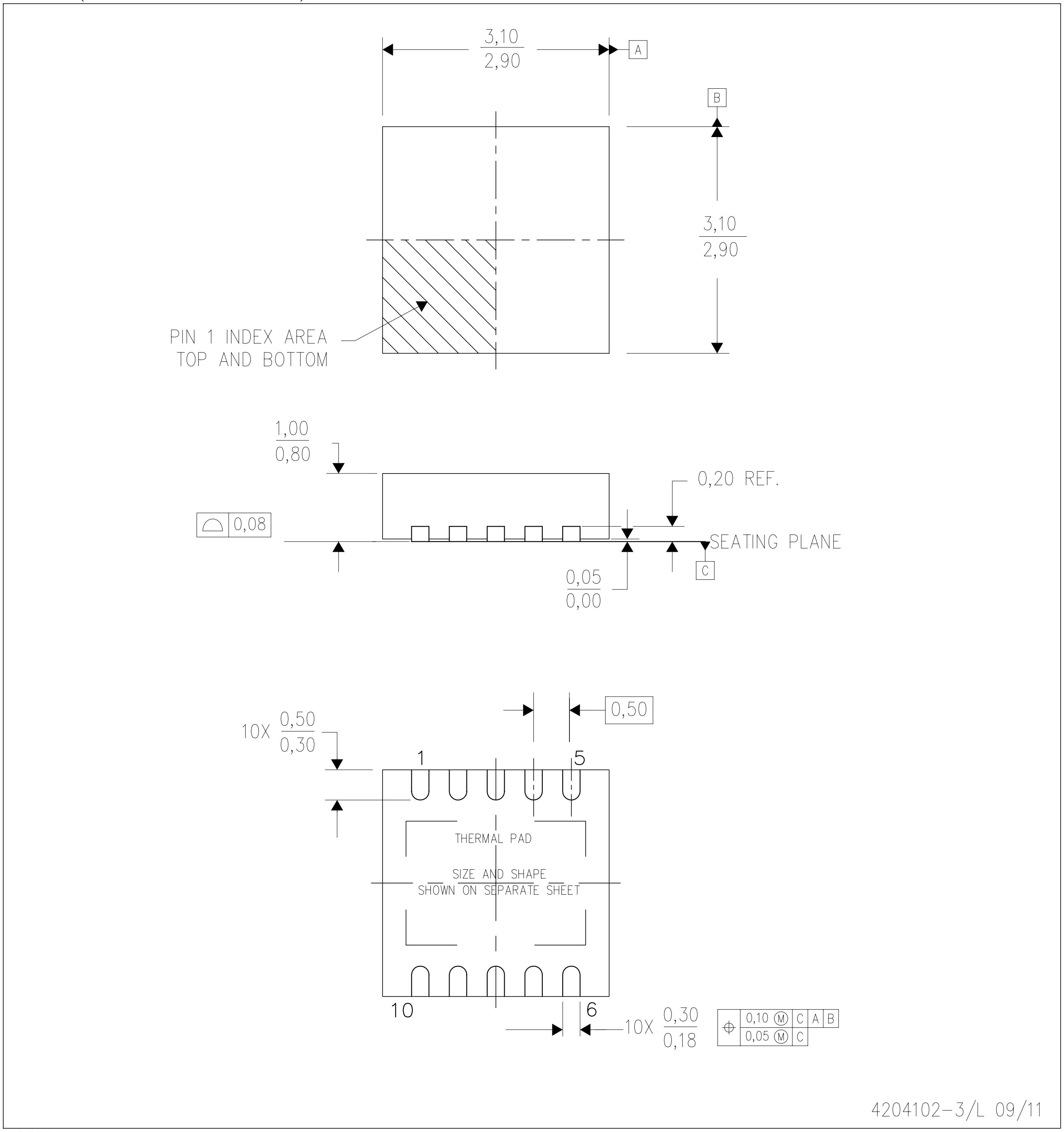
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5166DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
LM5166DRCT	VSON	DRC	10	250	210.0	185.0	35.0

DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

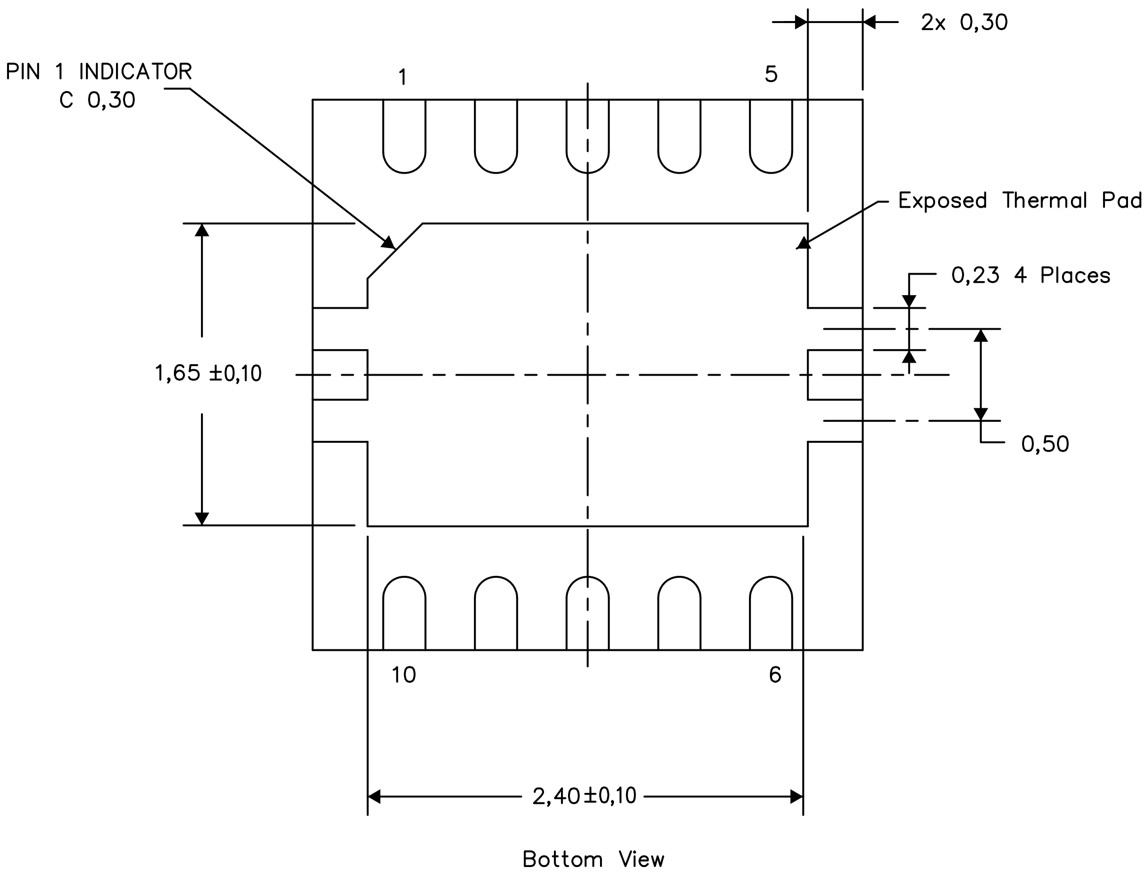
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

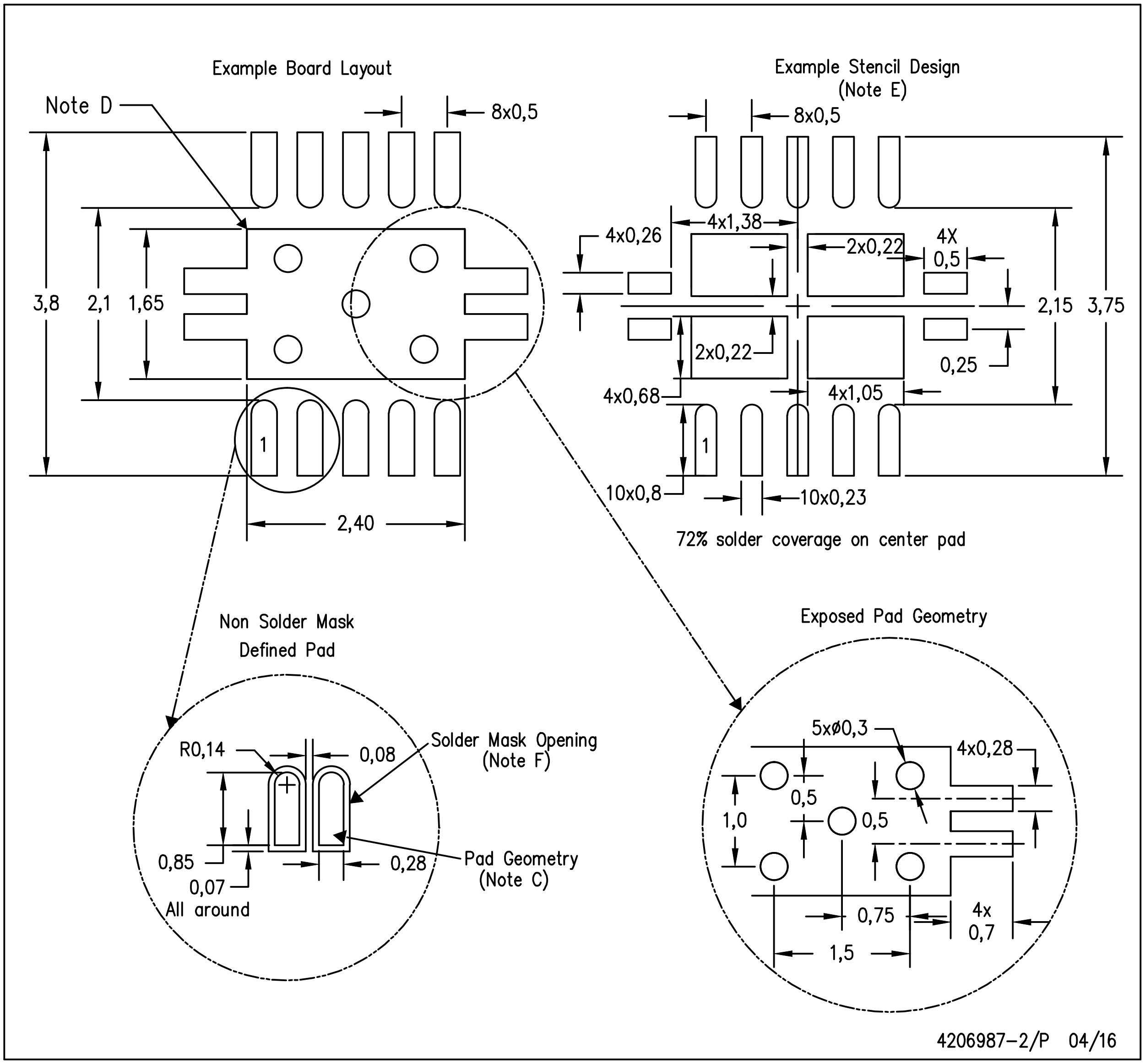


Exposed Thermal Pad Dimensions

4206565–3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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