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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2021	*	Initial Release

5 Description (continued)

The device is designed to power noise-sensitive components such as those found in high-speed communication, video, medical, or test and measurement applications. The very low $0.46\text{-}\mu\text{V}_{\text{RMS}}$ output noise and wideband PSRR (60 dB at 1 MHz) minimizes phase noise and clock jitter. These features maximize performance of clocking devices, DACs, and ADCs.

6 Pin Configuration and Functions

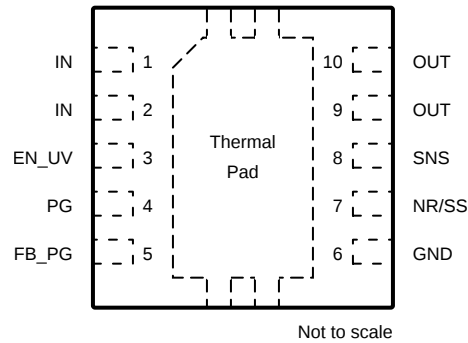


Figure 6-1. DSC Package, 10-Pin WSON (Top View)

Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
NAME	WSON		
EN_UV	3	I	Precision enable and under voltage lockout pin. This pin turns the LDO on and off. If $V_{EN_UV} \geq V_{EN_UV(HI)}$, the regulator is enabled. If $V_{EN_UV} \leq V_{EN_UV(LOW)}$, the regulator is disabled. The EN_UV pin does not incorporate an internal pulldown resistor to GND and must not be left floating. Use the precision enable circuit for this pin to set an external undervoltage lockout (UVLO) input supply voltage to turn on and off the device using a resistor divider between IN, EN_UV, and GND. See the Precision Enable (External UVLO) section for detail.
FB_PG	5	I	Power-good feedback pin. This pin has a dual function: this pin programs the output threshold for the PG pin and sets (adjusts) the factory-programmed current limit value specified in the Recommended Operating Conditions table to either 100%, 80%, or 60%. The parallel impedance formed by the resistor divider $R_{FB_PG(TOP)}$ and $R_{FB_PG(BOTTOM)}$ affects the current limit value. If this impedance is less than 10 k Ω , then the nominal factory-programmed, current-limit value is selected. If the input impedance is less than 50 k Ω , but greater than 10 k Ω , then 80% of the nominal factory-programmed current limit is selected. If the input impedance is less than 100 k Ω , but greater than 50 k Ω , then 60% of the nominal factory-programmed current limit is selected. Connect the $R_{FB_PG(TOP)}$ and $R_{FB_PG(BOTTOM)}$ resistors as indicated in the Adjusting the Factory-Programmed Current Limit section for proper operation of the LDO. Do not float this pin.
GND	6	G	Ground pin. Connect this pin to the device thermal pad and connect both this pin and the thermal pad to the ground on the board through a low-impedance connection.
IN	1, 2	I	Input voltage supply pin. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground as listed in the Recommended Operating Conditions table. Place the input capacitor as close to the IN and GND pins of the device as possible.
NR/SS	7	I	Output voltage set and noise-reduction pin. This pin is the input to the inverting terminal of the error amplifier. A resistor connected from this pin to GND sets the output voltage by the pin internal reference current $I_{NR/SS}$, $V_{OUT} = I_{NR/SS} \times R_{NR/SS}$. Connecting a capacitor from this pin to GND significantly reduces the device noise, limits the input inrush-current, and soft-starts the output voltage. Use the minimum value or larger capacitor from NR/SS to ground as listed in the Recommended Operating Conditions table and place the NR/SS capacitor as close to the NR/SS and GND pins of the device as possible.
OUT	9, 10	O	Regulated output pin. For best transient response, use the nominal value or larger capacitor from OUT to ground as listed in the Recommended Operating Conditions table. Place the out capacitor as close to the OUT and GND pins of the device as possible.
PG	4	O	Open-drain power-good indicator pin for the LDO output voltage. Use the minimum value or larger pullup resistor from PG to IN or the external rail as listed in the Recommended Operating Conditions table. If PG functionality is not used, leave this pin floating or connected to GND.
SNS	8	I	Output sense pin. This pin is the input to the noninverting terminal of the error amplifier. Kelvin connects the SNS pin through a low-impedance connection to the output capacitor and load for optimal transient performance. Do not float this pin.
Thermal pad		P	The thermal pad is electrically connected to the GND pin. Connect the thermal pad to a large-area GND plane for improved thermal performance.

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range and all voltages with respect to GND(unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	IN, PG, EN	−0.3	6.0	V
	IN, PG, EN (5% duty cycle, pulse duration ≤ 200 μs)	−0.3	6.0	
	PGFB	−0.3	1.5	
	OUT	−0.3	V _{IN} + 0.3	
	NR/SS, FB	−0.3	6.0	
Current	OUT	Internally limited		A
	PG (sink current into the device)		5	mA
Temperature	Operating junction, T _J	−55	150	°C
	Storage, T _{stg}	−55	150	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged device model (CDM), per per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V _{IN}	Input supply voltage range	1.7		5.7	V
V _{OUT}	Output voltage range	0		5.7	V
I _{OUT}	Output current	0		1	A
C _{IN}	Input capacitor	4.7	10	1000	μF
C _{OUT}	Output capacitor	4.7	10	1000	μF
C _{NR/SS}	Noise-reduction capacitor	0	4.7	100	μF
R _{PG}	Power-good pull-up resistance	10		100	kΩ
T _J	Junction temperature	−40		150	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7A94		UNIT
		DSC (WSON) ⁽²⁾	DSC (WSON) ⁽³⁾	
		10 PINS	10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	46.1	25.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	35.2	-	°C/W
R _{θJB}	Junction-to-board thermal resistance	19.1	-	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.5	0.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	19	11.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	3.9	-	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and ICPackage Thermal Metrics](#) application report.

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- (2) JEDEC Standard. (2s2p)
- (3) EVM model thermal model using JEDEC measurement methodology

ADVANCE INFORMATION

7.5 Electrical Characteristics

over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $V_{IN(NOM)} = V_{OUT(NOM)} + 0.5\text{ V}$, $V_{OUT(NOM)} = 3.3\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = 1.8\text{ V}$, $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR/SS} = 0\text{ nF}$, and PG pin pulled up to V_{IN} with 100 k-ohm (unless otherwise noted); typical values are at $T_J = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IN}	Input supply voltage range		1.7		5.7	V
V _{UVLO}	Input supply UVLO	V _{IN} rising, no load		1.6	1.7	V
V _{HYS(UVLO)}	Input supply UVLO hysteresis	No load		53		mV
I _{NR/SS}	NR/SS current pin	V _{IN} = V _{IN(MIN)} + 0.2 V, I _{LOAD} = 1 mA, V _{OUT} = 1.5 V		150		μA
		V _{IN(MIN)} ≤ V _{IN} ≤ 5.5 V, V _{OUT(MIN)} ≤ V _{OUT} < 1.2 V, 100 μA ≤ I _{OUT} ≤ 1 A	-1.5		1.5	%
		V _{IN(MIN)} ≤ V _{IN} ≤ 5.5 V, 1.2 V ≤ V _{OUT} ≤ 5 V, 100 μA ≤ I _{OUT} ≤ 1 A	-1		1	%
	NR/SS fast startup charging current	V _{NR/SS} = GND, V _{IN} ≥ 2.5 V, V _{PG_FB} < 0.2 V, I _{OUT} = 0 mA		2		mA
		V _{NR/SS} = GND, V _{IN} ≥ 1.7 V, V _{PG_FB} < 0.2 V, I _{OUT} = 0 mA		1.4		
V _{OUT}	Output voltage range		0		5.7 - V _{DO}	V
V _{OS}	Output offset voltage (V _{NR/SS} - V _{OUT})	V _{IN} = 1.7 V, V _{OUT} ≥ 1.2 V, I _{OUT} = 1 mA	-1		1	mV
		1.7 V ≤ V _{IN} ≤ 5.7 V, 1.2 V ≤ V _{OUT} ≤ 5.5 V - V _{DO} , 1 mA ≤ I _{OUT} ≤ 1 A	-2		2	
		1.7 V ≤ V _{IN} ≤ 5.7 V, 0.4 V < V _{OUT} < 1.2 V, 1 mA ≤ I _{OUT} ≤ 1 A	-5		5	
ΔV _{OUT(ΔV_{IN})}	Line regulation: ΔI _{NR/SS}	0.4 V ≤ V _{OUT} < 1.2 V, I _{OUT} = 1 mA V _{IN(NOM)} (= V _{OUT} + 0.5 V) to V _{IN(MAX)}		-2.25		nA/V
		V _{OUT} = 1.2 V & 3.3 V, I _{OUT} = 1mA V _{IN(NOM)} (= V _{OUT} + 0.5V) to V _{IN(MAX)}		-4.5		
	Line regulation: ΔV _{OS}	0.4 V ≤ V _{OUT} < 1.2 V, I _{OUT} = 1 mA V _{IN(NOM)} (= V _{OUT} + 0.5 V) to V _{IN(MAX)}		1.0		μV/V
		V _{OUT} = 1.2 V & 3.3 V, I _{OUT} = 1 mA V _{IN(NOM)} (= V _{OUT} + 0.5 V) to V _{IN(MAX)}		1.1		
ΔV _{OUT(ΔI_{OUT})}	Load regulation: ΔI _{NR/SS} ⁽²⁾	V _{IN} = 1.7 V, V _{OUT} = 1.2 V, 1 mA ≤ I _{OUT} ≤ 1 A		7		nA
		V _{IN} = 3.8 V, V _{OUT} = 3.3 V, 1 mA ≤ I _{OUT} ≤ 1 A		5		
		V _{IN} = 5.7 V, V _{OUT} = 5.1 V, 1 mA ≤ I _{OUT} ≤ 1 A		5		
	Load regulation: ΔV _{OS} ⁽²⁾	V _{IN} = 1.7 V, V _{OUT} = 1.2 V, 1 mA ≤ I _{OUT} ≤ 1 A		0.023	0.7	mV
		V _{IN} = 3.8 V, V _{OUT} = 3.3 V, 1 mA ≤ I _{OUT} ≤ 1 A		0.023	0.7	
		V _{IN} = 5.7 V, V _{OUT} = 5.1 V, 1 mA ≤ I _{OUT} ≤ 1 A		0.023	0.7	
	Change in I _{NR/SS} vs V _{NR/SS}	1.5 V ≤ V _{NR/SS} ≤ 5 V, V _{IN} = V _{IN_MAX} , I _{OUT} = 1 mA		11		nA
	Change in V _{OS} vs V _{NR/SS}			0.001		mV
	Change in I _{NR/SS} vs V _{NR/SS}	0V ≤ V _{NR/SS} ≤ 1.5 V, V _{IN} = V _{IN_MAX} , I _{OUT} = 1 mA		-7		nA
	Change in V _{OS} vs V _{NR/SS}	V _{NR/SS} = 0 V to 1.5 V, V _{IN} = V _{IN_MAX} , I _{OUT} = 1 mA		-0.002		mV
V _{DO}	Dropout voltage ⁽³⁾	1.7 V ≤ V _{IN} < 2.0 V, I _{OUT} = 1 mA, V _{OUT} = 99% x V _{OUT_NOM}		180	275	mV
		1.7 V ≤ V _{IN} < 2.0 V, I _{OUT} = 1 A, V _{OUT} = 99% x V _{OUT_NOM}		210	280	
		V _{IN} ≥ 2.0 V, I _{OUT} = 1 mA, V _{OUT} = 99% x V _{OUT_NOM}		140	230	
		V _{IN} ≥ 2.0 V, I _{OUT} = 1 A, V _{OUT} = 99% x V _{OUT_NOM}		150	240	

7.5 Electrical Characteristics (continued)

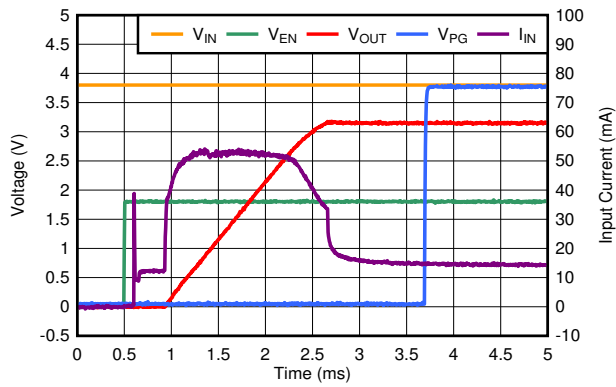
over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $V_{IN(NOM)} = V_{OUT(NOM)} + 0.5\text{ V}$, $V_{OUT(NOM)} = 3.3\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = 1.8\text{ V}$, $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR/SS} = 0\text{ nF}$, and PG pin pulled up to V_{IN} with 100 k-ohm (unless otherwise noted); typical values are at $T_J = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIM}	V_{OUT} forced at $0.9 \times V_{OUT(NOM)}$, $V_{IN} = V_{OUT(NOM)} + 200\text{ mV}$ or $V_{IN} = V_{IN_MIN}$ whichever is greater, $V_{OUT(NOM)} \geq 1.2\text{ V}$, $R_{PGFB-to-GND} \leq 12.5\text{ k}\Omega$ ($\pm 1\%$)	1.2	1.3	1.4	A
	V_{OUT} forced at $0.9 \times V_{OUT(NOM)}$, $V_{IN} = V_{OUT(NOM)} + 200\text{ mV}$ or $V_{IN} = V_{IN_MIN}$ whichever is greater, $V_{OUT(NOM)} \geq 1.2\text{ V}$, $R_{PGFB-to-GND} = 50\text{ k}\Omega$ ($\pm 1\%$)	0.96	1.04	1.12	A
	V_{OUT} forced at $0.9 \times V_{OUT(NOM)}$, $V_{IN} = V_{OUT(NOM)} + 200\text{ mV}$ or $V_{IN} = V_{IN_MIN}$ whichever is greater, $V_{OUT(NOM)} \geq 1.2\text{ V}$, $R_{PGFB-to-GND} = 100\text{ k}\Omega$ ($\pm 1\%$)	0.72	0.78	0.84	A
ΔI_{SC}	Short-circuit Current Limit Variation ⁽⁴⁾ $V_{IN} = V_{OUT(NOM)} + 200\text{ mV}$ or $V_{IN} = V_{IN_MIN}$ whichever is greater, $V_{OUT} = 0\text{ V}$		1.85		%
I_{GND}	GND pin current $V_{IN} = 5.5\text{ V}$, $I_{OUT} = 0.1\text{ mA}$	8	15	22	mA
	$V_{IN} = 1.7\text{ V}$, $I_{OUT} = 1\text{ A}$, $V_{OUT} = 1.2\text{ V}$	34	41	51	
I_{SDN}	Shutdown GND pin current PG = (open), $V_{IN} = 5.5\text{ V}$, $V_{EN} = 0.4\text{ V}$		0.5	100	μA
I_{EN}	EN pin current $V_{IN} = 5.7\text{ V}$, $0\text{ V} \leq V_{EN} \leq 5.5\text{ V}$	–1		1	μA
$V_{IH(EN)}$	EN trip point rising (Turn-On) $V_{IN} = 1.7\text{ V}$, no load	1.20	1.22	1.25	V
$V_{IL(EN)}$	EN trip point hysteresis $V_{IN} = 1.7\text{ V}$, no load		110		mV
t_{PGDH}	PG delay time rising Time from programmed PG threshold% to 20% of PG		1.1		ms
t_{PGDL}	PG delay time falling Time from 90% of V_{OUT} to 80% of PG		3		μs
V_{FB_PG}	FB_PG pin trip point $1.7\text{ V} \leq V_{IN} \leq 5.7\text{ V}$	0.19	0.2	0.21	V
$V_{HYS(PG)}$	FB_PG pin hysteresis $1.7\text{ V} \leq V_{IN} \leq 5.7\text{ V}$		6		mV
$V_{OL(PG)}$	PG pin low-level output voltage $V_{IN} = 1.7\text{ V}$, $V_{OUT} < V_{IT(PG)}$, $I_{PG} = -1\text{ mA}$ (current into device)			0.4	V
$I_{LKG(PG)}$	PG pin leakage current $V_{IN} = 5.7\text{ V}$, $V_{OUT} > V_{IT(PG)}$, $V_{PG} = 5.5\text{ V}$			1	μA
I_{FB_PG}	FB_PG pin leakage current $V_{IN} = 5.7\text{ V}$, $V_{FB} = 0.2\text{ V}$	–100		100	nA
PSRR	Power-supply ripple rejection $f = 1\text{ MHz}$, $V_{IN} = 3.8\text{ V}$, $V_{OUT(NOM)} = 3.3\text{ V}$, $I_{OUT} = 750\text{ mA}$, $C_{NR/SS} = 4.7\text{ }\mu\text{F}$		75		dB
V_n	Output noise voltage BW = 10 Hz to 100 kHz, $V_{IN} \leq 5.7\text{ V}$, $V_{OUT(NOM)} = 1.2\text{ V}$, $I_{OUT} = 1.0\text{ A}$, $C_{NR/SS} = 4.7\text{ }\mu\text{F}$		0.48		μV_{RMS}
	BW = 10 Hz to 100 kHz, $V_{IN} = 1.8\text{ V}$, $V_{OUT(NOM)} = 0.8\text{ V}$, $I_{OUT} = 1.0\text{ A}$, $C_{NR/SS} = 4.7\text{ }\mu\text{F}$		0.8		
	Noise spectral density $f = 100\text{ Hz}$, $V_{IN} \leq 5.7\text{ V}$, $V_{OUT(NOM)} = 1.2\text{ V}$, $I_{OUT} = 1.0\text{ A}$, $C_{NR/SS} = 4.7\text{ }\mu\text{F}$		6		nV/ $\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$, $V_{IN} \leq 5.7\text{ V}$, $V_{OUT(NOM)} = 1.2\text{ V}$, $I_{OUT} = 1.0\text{ A}$, $C_{NR/SS} = 4.7\text{ }\mu\text{F}$		1.3		
	$f = 10\text{ kHz}$, $V_{IN} \leq 5.7\text{ V}$, $V_{OUT(NOM)} = 1.2\text{ V}$, $I_{OUT} = 1.0\text{ A}$, $C_{NR/SS} = 4.7\text{ }\mu\text{F}$		1.1		
R_{diss}	Output active discharge resistance $V_{IN} = 1.7\text{ V}$, $V_{EN} = \text{GND}$		155		Ω
TSD(shutdown)	Thermal shutdown temperature Shutdown, temperature increasing		175		$^{\circ}\text{C}$
TSD(reset)	Thermal shutdown reset temperature Reset, temperature decreasing		160		

- (1) When the device is connected to an external feedback resistor at the FB pin, external resistor tolerances are not included.
- (2) The device is not tested under conditions where $V_{IN} > V_{OUT} + 2.5\text{ V}$ and $I_{OUT} = 1\text{ A}$ because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.
- (3) Measured when output voltage drops 1% below targeted value.
- (4) Brickwall filter: $I_{LIMIT_ \%} = (I_{SC} - I_{LIMIT_ @0.9 \times V_{OUT}}) / I_{LIMIT_ @0.9 \times V_{OUT}} \times 100$.

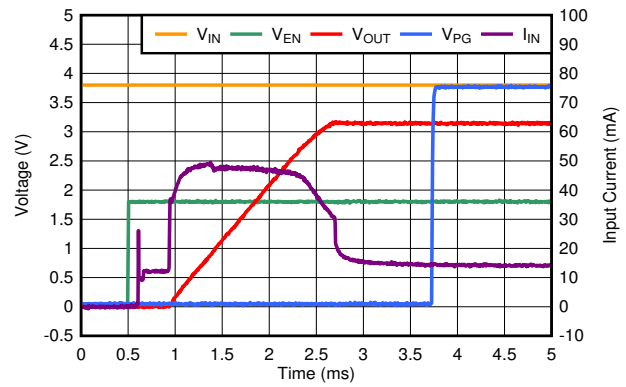
7.6 Typical Characteristics

$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$, $V_{EN} = 1.8\text{ V}$, $C_{IN} = 10\text{ }\mu\text{F}$, $C_{NR/SS} = 4.7\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, and $I_{OUT} = 1\text{ mA}$ (unless otherwise noted); typical values are at $T_J = 25^\circ\text{C}$



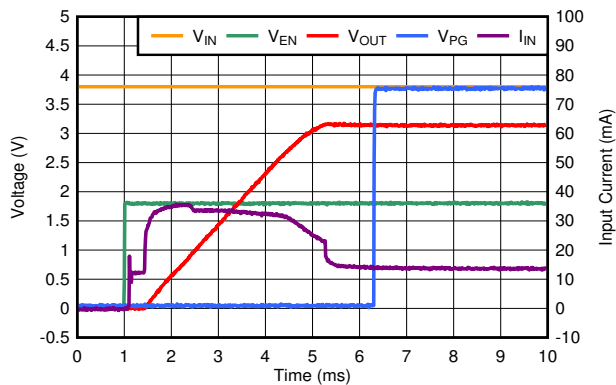
$C_{IN} = 0\text{ }\mu\text{F}$, $C_{NR/SS} = 0.47\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $I_{OUT} = 0\text{ mA}$

Figure 7-1. Start-Up Time and Inrush Current



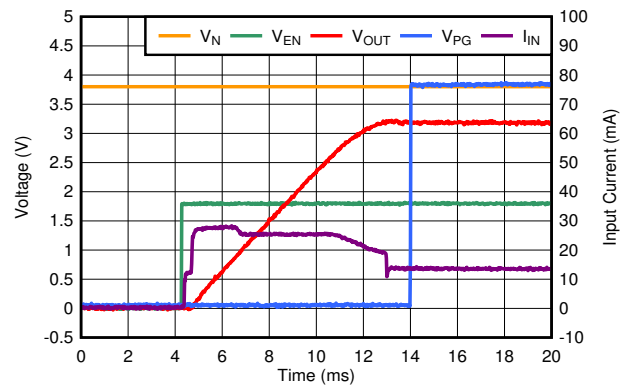
$C_{IN} = 0\text{ }\mu\text{F}$, $C_{NR/SS} = 1\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $I_{OUT} = 0\text{ mA}$

Figure 7-2. Start-Up Time and Inrush Current



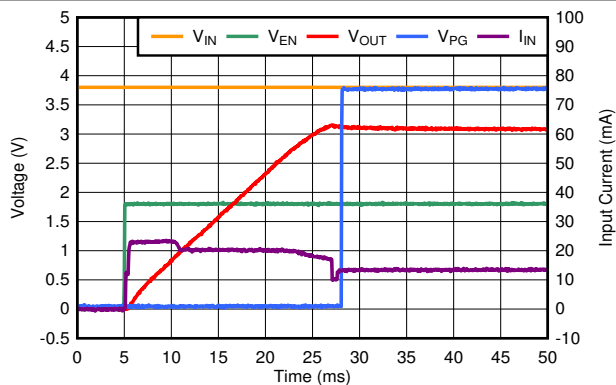
$C_{IN} = 0\text{ }\mu\text{F}$, $C_{NR/SS} = 2.2\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $I_{OUT} = 0\text{ mA}$

Figure 7-3. Start-Up Time and Inrush Current



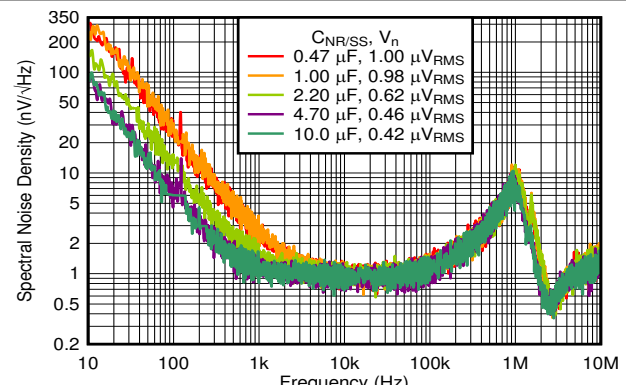
$C_{IN} = 0\text{ }\mu\text{F}$, $C_{NR/SS} = 4.7\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $I_{OUT} = 0\text{ mA}$

Figure 7-4. Start-Up Time and Inrush Current



$C_{IN} = 0\text{ }\mu\text{F}$, $C_{NR/SS} = 10\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $I_{OUT} = 0\text{ mA}$

Figure 7-5. Start-Up Time and Inrush Current

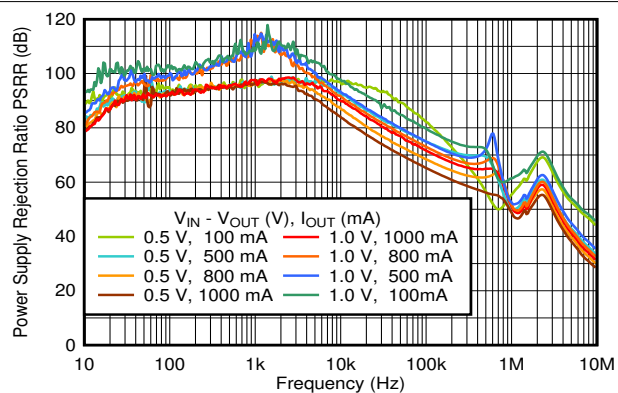


$C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$, $I_{OUT} = 500\text{ mA}$, $BW = 10\text{ Hz to }100\text{ kHz}$

Figure 7-6. Output Noise vs $C_{NR/SS}$

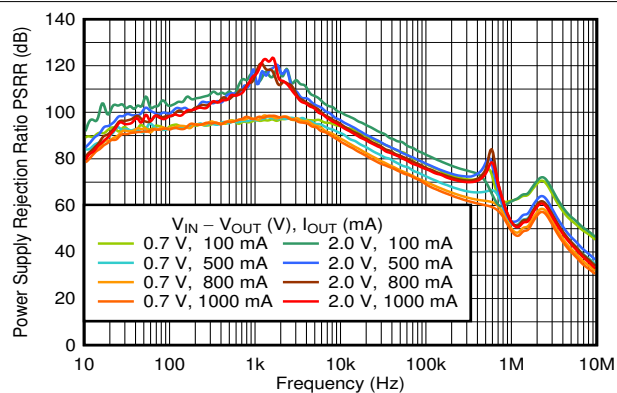
7.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$, $V_{EN} = 1.8\text{ V}$, $C_{IN} = 10\text{ }\mu\text{F}$, $C_{NR/SS} = 4.7\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, and $I_{OUT} = 1\text{ mA}$ (unless otherwise noted); typical values are at $T_J = 25^\circ\text{C}$



$C_{IN} = 0\text{ }\mu\text{F}$, $V_{OUT} = 3.3\text{ V}$, $C_{NR/SS} = 4.7\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$

Figure 7-7. PSRR vs Frequency, V_{DO} , and I_{OUT}



$C_{IN} = 0\text{ }\mu\text{F}$, $V_{OUT} = 3.3\text{ V}$, $C_{NR/SS} = 4.7\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$

Figure 7-8. PSRR vs Frequency, V_{DO} , and I_{OUT}

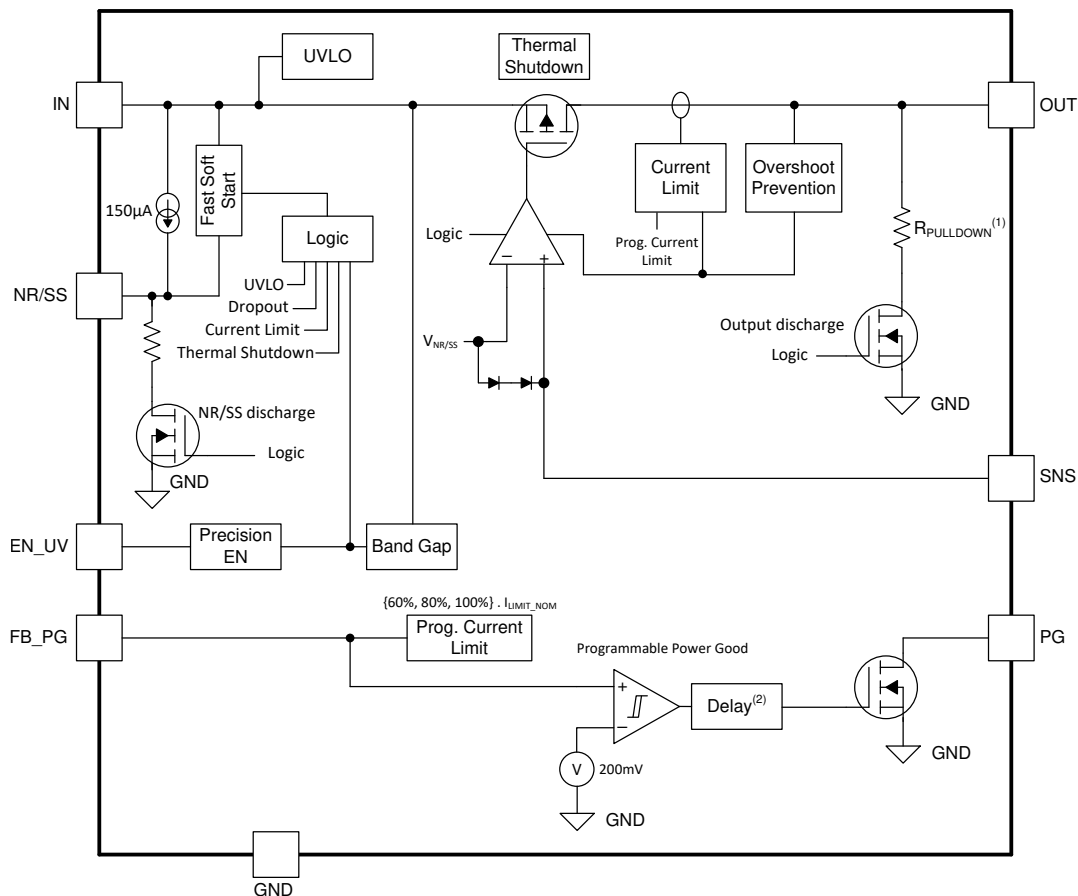
8 Detailed Description

8.1 Overview

The TPS7A94 is an ultra-low noise ($0.46 \mu\text{V}_{\text{RMS}}$ over 10-Hz to 100-kHz bandwidth), ultra-high PSRR ($> 60 \text{ dB}$ to 2 MHz), high-accuracy (1%), low-dropout (LDO) linear voltage regulator with an input range of 1.7 V to 5.7 V and an output voltage range from 0 V to $V_{\text{IN}} - V_{\text{DO}}$. This device is an LDO regulator that uses innovative circuitry to achieve wide-bandwidth and high loop gain, resulting in ultra-high PSRR even with very low operational headroom ($V_{\text{IN}} - V_{\text{OUT}}$). At a high level, the device has two main components, the current reference followed by a unity-gain LDO. The ultra-low noise current reference, $150 \mu\text{A}$ typical, is used in conjunction with an external resistor ($R_{\text{NR/SS}}$) to program (set) the output voltage. This process allows the output voltage range to be set from 0 V to $V_{\text{IN}} - V_{\text{DO}}$. To achieve ultra-low noise, an external capacitor $C_{\text{NR/SS}}$ (typically $4.7 \mu\text{F}$) is placed in parallel to the $R_{\text{NR/SS}}$ resistor used to set the output voltage. This unity-gain LDO provides ultra-high PSRR over a wide frequency range without compromising load and line transients.

This regulator offers programmable current limit, thermal protection, is fully specified from -40°C to $+125^\circ\text{C}$, and is offered in a 10-pin WSON, 3-mm \times 3-mm thermally efficient package.

8.2 Functional Block Diagram



- (1) See (R_{PULLDOWN}) output active discharge resistance value in *Electrical Characteristics* table
(2) See Delay value in *Electrical Characteristics* table

8.3.1 Output Voltage Setting and Regulation

The low output impedance of an LDO comes from the combination of the output capacitor and pass element. The pass element also presents a high input impedance to the input source while operating as a current source. A positive LDO can only source current because of the class-B architecture.



Figure 8-1. Simplified Regulation Circuit

8.3.2 Ultra-Low Noise and Ultra-High Power-Supply Rejection Ratio (PSRR)

The device architecture features a highly accurate, ultra-low noise current reference followed by a state-of-the-art error amplifier (1.1 nV/ $\sqrt{\text{Hz}}$ at 10 kHz noise) with an ultra-high PSRR (60 dB > 1 MHz) comparable to, if not better than, that of a precision amplifier. The unity-gain configuration of this device eliminates the high RMS noise in traditional linear regulators resulting from the feedback resistor divider gaining factor. Additionally, in a unity-gain configuration, the device output noise is independent of the set output voltage. Additional noise reduction can be achieved by placing multiple TPS7A94 LDOs in parallel.

8.3.3 Programmable Current Limit and Power-Good Threshold

The value for the factory-programmed, brick-wall current limit for this device can be programmed to either 100%, 80%, or 60% of its value by setting the input impedance for the FB_PG pin. Similarly, the power-good indication threshold can also be adjusted to assert when the output voltage reaches 85% to 95% by changing the FB_PG resistor divider ratio; see [Table 9-1](#) for details.

8.3.4 Programmable Soft Start (NR/SS Pin)

The device features a programmable, monotonic, voltage-controlled, soft-start circuitry that uses the C_{NR/SS} capacitor to minimize inrush current into the output capacitor and the load during start up. This circuitry can also reduce the start-up time for some applications that require the output voltage to reach at least 90% of its set value for fast system start up. See the [Precision Enable and UVLOs](#) section for more details.

8.3.5 Precision Enable and UVLOs

The device features a precision enable circuit that allows a simple sequencing of multiple power supplies with a resistor divider from another supply. This enable circuit can be used to set an external UVLO voltage at which the device is enabled using a resistor divider on the EN_UV pin; see the [Precision Enable \(External UVLO\)](#) section for more details.

The device incorporates an input supply voltage undervoltage lockout (V_{UVLO}) circuit that prevents the regulator from turning on when the input voltage is not high enough to properly bias the LDO internal circuitry.

8.3.6 Thermal Shutdown Protection (T_{SD})

A thermal shutdown protection circuit disables the LDO when the junction temperature (T_J) of the pass transistor rises to T_{SD(shutdown)} (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to T_{SD(reset)} (typical). The thermal time constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes. For reliable operation, limit the junction temperature to the maximum listed in the [Recommended Operating Conditions](#) table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

8.3.7 Active Discharge

The device also incorporates an internal pulldown MOSFET that connects a resistor (R_{PULLDOWN}) from OUT to ground when the device is disabled to actively discharge the output capacitor. The active discharge circuit is activated by driving the EN_UV pin below the V_{EN(LOW)} threshold or by the voltage on the IN pin falling below the undervoltage lockout V_{UVLO} threshold but still higher than or equal to a diode-drop voltage to drive the MOSFET gate.

8.4 Device Functional Modes

Table 8-1 shows the conditions that lead to the different modes of operation. See the [Electrical Characteristics](#) table for parameter values.

Table 8-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN_UV}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN_UV} > V_{EN_UV(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN_UV} > V_{EN_UV(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$ or $V_{IN} < V_{OUT} + 300$ mV or $V_{IN} < V_{NR/SS} + 20$ mV	$V_{EN_UV} < V_{EN_UV(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

8.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD(shutdown)}$)
- The voltage on the EN_UV pin has previously exceeded the $V_{EN_UV(HI)}$ threshold voltage and has not yet decreased to less than the $V_{EN_UV(LOW)}$ falling threshold

8.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

While in dropout, if a heavy load transient event forces $V_{IN} < V_{OUT(NOM)} + 300$ mV or $V_{IN} < V_{NR/SS} + 20$ mV; the device restarts to prevent the output voltage from overshooting to protect the device and load.

When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

8.4.3 Disabled

The output of the device can be shutdown by forcing the voltage of the EN_UV pin to less than the $V_{EN_UV(LOW)}$ threshold (see the [Electrical Characteristics](#) table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground when the IN pin voltage is higher than or equal to a diode-drop voltage.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and how to best implement them to achieve a reliable design.

9.1.1 Output Voltage Restart (Overshoot Prevention Circuit)

Linear regulators with a very fast response time with wide bandwidth suffer from an undesirable excessive overshooting of the output voltage during restart events when the $C_{NR/SS}$ and C_{OUT} capacitors are not fully discharged. As shown in [Figure 9-1](#), this undesirable behavior is mitigated in this device by implementing sensitive circuitry consisting of two comparators that are OR-gated together to detect when the input voltage is either 20 mV (typical) lower than the $V_{NR/SS}$ reference voltage or 300 mV (typical) lower than V_{OUT} .

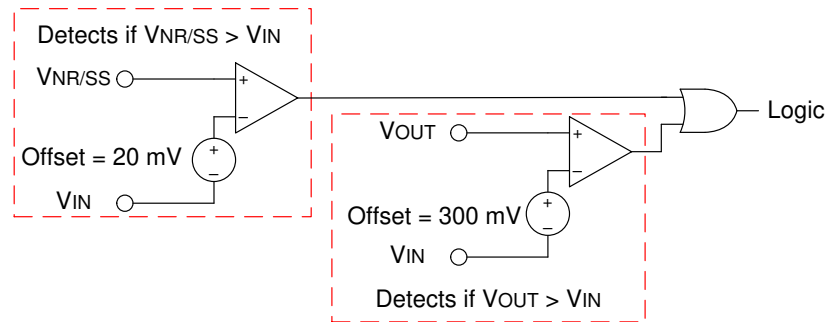


Figure 9-1. Overshoot Prevention Circuit

When the device is operating in dropout, transient events (such as an input voltage brownout, heavy load transient, or short-circuit event) can force the device into a reversed bias condition where the input voltage is either 20 mV (typical) lower than the $V_{NR/SS}$ reference voltage or 300 mV (typical) lower than V_{OUT} . The output overshoot prevention circuit can be triggered, as shown in [Figure 9-2](#), thus forcing the device to shutdown and restart and preventing output voltage overshooting. If the device is still operating in dropout and the error condition that triggered this circuit is still present, an additional restart can occur until these conditions are removed or the device is no longer in dropout. The restart always occurs from a discharged state and always has the same characteristics as the initial LDO power-up, so it is predictable for; start-up time, V_{OUT} ramp-rate, and V_{OUT} monotonicity.

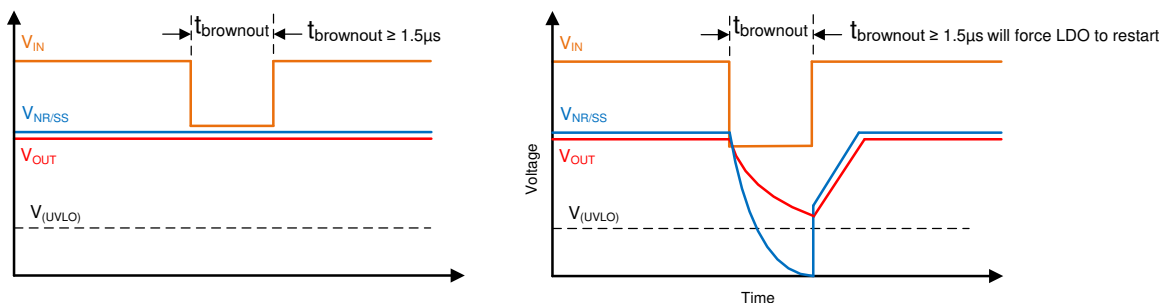


Figure 9-2. Device Behavior in Dropout

As shown in Figure 9-3, ripple present on the IN voltage during power-supply ramp up and ramp down must be less than $V_{DO(max)}$ of the device because higher voltage ripple can trigger the overshoot prevention circuit.

The precision EN_UV pin can be used to set an external undervoltage lockout input voltage to enable the LDO above a set output voltage with sufficient operating headroom to prevent this behavior.

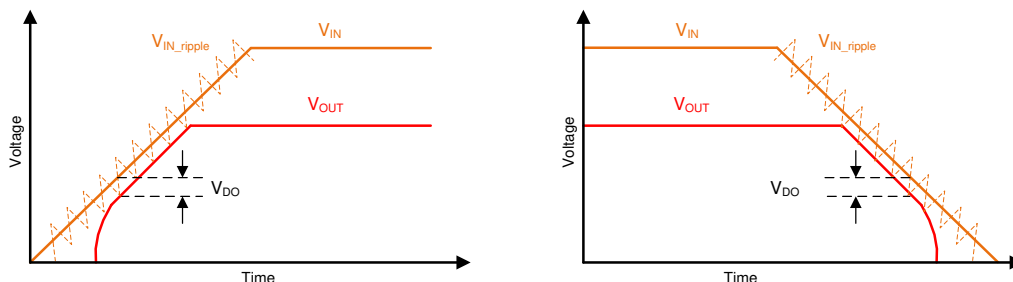


Figure 9-3. Device Start-Up Behavior in Dropout

The overshoot prevention circuit is implemented to ensure a predictable start up and shutdown of the device without output overshoot if the EN_UV external UVLO is not used as described in this section. This circuit can be prevented from triggering by:

1. Use an input supply capable of handling heavy load transients by increasing the input capacitor to a larger value.
2. Increase the operating headroom between V_{IN} and V_{OUT} (for example, when using a battery as an input supply to ensure that V_{IN} stays higher than V_{OUT} even when the battery is near its full discharge state).
3. Use an input supply with a ramp-rate faster than the set output voltage time constant formed by $C_{NR/SS} \parallel R_{NR/SS}$.
4. Discharge the input supply slower than the discharge time formed by $C_{OUT} \parallel (Load + R_{PULLDOWN})$.

9.1.2 Precision Enable (External UVLO)

The precision enable circuit is used to turn the device on and off. This circuit can be used to set an external undervoltage lockout (UVLO) voltage, as shown in Figure 9-4, to turn on and off the device using a resistor divider between IN, EN_UV, and GND.

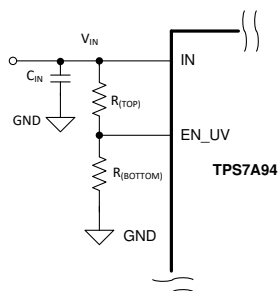


Figure 9-4. Precision EN Used as External UVLO

This external UVLO solution is used to prevent the device from turning on when the input supply voltage is not high enough and can place the device in dropout operation. This solution also allows simple sequencing of multiple power supplies with a resistor divider from another supply. Another benefit from using a resistor divider to enable or disable the device is that the EN_UV pin is never left floating because this pin does not have an internal pulldown resistor. However, a zener diode may be needed between the EN_UV pin and ground to comply with the absolute maximum ratings on this pin.

Use [Equation 1](#) and [Equation 2](#) to determine the correct resistor values.

$$V_{ON} = V_{OFF} \times [(V_{EN_UV} + V_{EN_UV(HYS)}) / V_{EN_UV}] \quad (1)$$

$$R_{(TOP)} = R_{(BOTTOM)} \times (V_{OFF} / V_{EN_UV} - 1) \quad (2)$$

where:

1. V_{OFF} is the input voltage where the regulator shuts off
2. V_{ON} is the voltage where the regulator turns on

9.1.3 Undervoltage Lockout (UVLO) Operation

The IN pin UVLO circuit makes sure that the device remains disabled before the input supply reaches the minimum operational voltage range, and that the device shuts down when the input supply falls too low.

The UVLO circuit has a minimum response time of several microseconds to fully assert. During this time, a downward line transient below approximately 0.8 V causes the input supply UVLO to assert for a short time. However, the UVLO circuit does not have enough stored energy to fully discharge the internal circuits inside of the device. When the UVLO circuit does not fully discharge, the internal circuits of the output are not fully disabled.

The effect of the downward line transient can trigger the overshoot prevention circuit and can be easily mitigated by using the solution proposed in [Precision Enable \(External UVLO\)](#).

[Figure 9-5](#) shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following regions:

- Region A: The device does not turn on until the input reaches the UVLO rising threshold.
- Region B: Normal operation with a regulated output.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device is still enabled.
- Region D: Normal operation with a regulated output.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached by the input voltage and a normal start up then follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

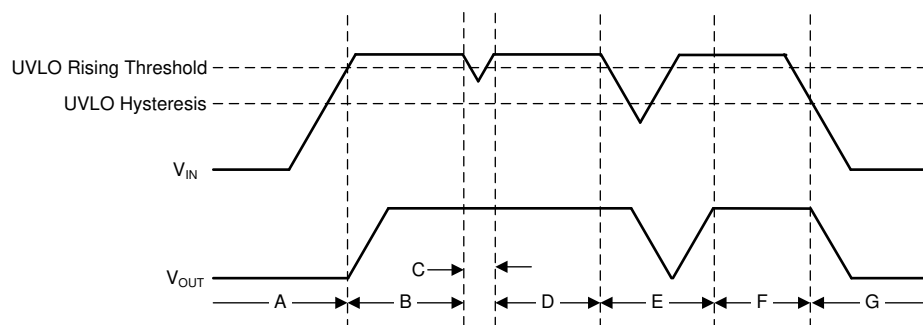


Figure 9-5. Typical UVLO Operation

9.1.4 Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the minimum voltage difference between the input and output voltage ($V_{DO} = V_{IN} - V_{OUT}$) that is required for regulation. When V_{IN} drops to or below the set V_{DO} for the given load current, the device functions as a resistive switch and does not regulate output voltage. While the device is operating in dropout, the output voltage tracks the input voltage and the dropout voltage (V_{DO}) is proportional to the output current because the device is operating as a resistive switch. As mentioned in the [Output Voltage Restart \(Overshoot Prevention Circuit\)](#) section, transient events such as an input voltage

brownout, heavy load transient, or short-circuit event can trigger the overshoot prevention circuit. Operating the device at or near dropout significantly degrades the device transient performance and PSRR and can also trigger the overshoot prevention circuit. Maintaining sufficient V_{DO} significantly improves the device transient performance and PSRR, and prevents the overshoot prevention circuit from triggering.

On this device, the pass element is not the limiting factor because the internal current source ($I_{NR/SS}$) becomes saturated faster than the pass element, resulting in a constant dropout voltage with regards to the output current.

9.1.5 Adjusting the Factory-Programmed Current Limit

The current limit for this device is a brick-wall scheme and the factory-programmed current limit value can be programmed to a lower value (such as 80% or 60% of its default value of 100%), as specified in the [Recommended Operating Conditions](#) table. This adjustment can be done by changing the input impedance of the FB_PG pin represented by the parallel resistance of $R_{FB_PG(TOP)} \parallel R_{FB_PG(BOTTOM)}$. The FB_PG pin has dual functionality: adjusting the I_{CL} and setting the power-good (PG) assert threshold.

Prior to device start up, the input impedance of the FB_PG pin is sampled and the I_{CL} value is adjusted based on the input impedance. [Table 9-1](#) lists the recommended PG_FB pin top and bottom resistor values needed to properly adjust the I_{CL} value to the required application level.

Table 9-1. Programmable Current Limit Voltage-Divider Current Settings

NOMINAL OUTPUT VOLTAGE (V)	$R_{FB_PG(BOTTOM)}$ (k Ω)	$R_{FB_PG(TOP)}$ (k Ω)	I_{CL} SETTING (%)	PG THRESHOLD (%)
$V_{OUT(nom)} = 1.2V$	12.4	51.4	100	85
	49.9	205	80	85
	100	410	60	85
$V_{OUT(nom)} = 3.3V$	12.4	187	100	95
	49.9	734	80	95
	100	1467	60	95
$V_{OUT(nom)} = 5.1V$	12.4	290	100	95
	49.9	1162	80	95
	100	2322	60	95

[Equation 3](#) can also be used to calculate the $R_{FB_PG(TOP)}$ and $R_{FB_PG(BOTTOM)}$ resistor values:

$$R_{FB_PG(TOP)} = R_{FB_PG(BOTTOM)} \times (V_{OUT(nom)} / V_{FB_PG(typ)} - 1) \quad (3)$$

Note

For this feature to be fully operational, the following two conditions must be true:

1. The V_{FB_PG} pin voltage set by the $R_{FB_PG(TOP)}$ and $R_{FB_PG(BOTTOM)}$ resistors from $V_{OUT(nom)}$ must be within $(V_{IN} - V_{DO})$ to the 0.2-V voltage range.
2. Set the output voltage ≥ 1.2 V.

Figure 9-6 shows the different I_{CL} settings for a nominal 3.3-V output voltage.

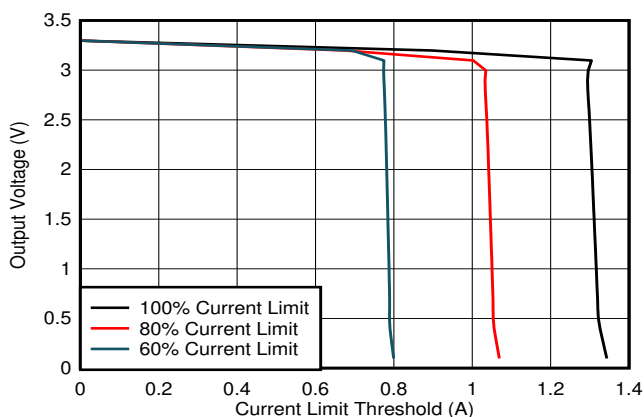


Figure 9-6. Programmable Current Limit Behavior (Typical) for a 3.3-V_{OUT(nom)}

9.1.6 Power-Good Feedback (FB_PG Pin) and Power-Good Threshold (PG Pin)

Note

For proper device operation, the resistor divider network input to the FB_PG pin must be connected. The FB_PG pin must not be left floating because this pin represents an analog input to the device internal logic and its input impedance is sampled during device start up.

To properly select the values of the $R_{FB_PG(TOP)}$ and $R_{FB_PG(BOTTOM)}$ resistors, see the [Adjusting the Factory-Programmed Current Limit](#) section for detailed explanation and calculation. As previously mentioned, the FB_PG pin has a dual purpose: to program the PG threshold assert voltage and adjust I_{CL} .

The $R_{FB_PG(TOP)}$ and $R_{FB_PG(BOTTOM)}$ resistor divider ratio is used to set the power-good assert threshold voltage between 70% to 90% of the V_{FB_PG} voltage specified in the [Recommended Operating Conditions](#) table. Setting the PG threshold based off the V_{FB_PG} voltage sets the PG to assert when the output voltage reaches the corresponding percentage level of V_{FB_PG} because V_{FB_PG} is a scaled version of the output voltage. Figure 9-7 shows the internal circuitry for both the FB_PG and PG pins.

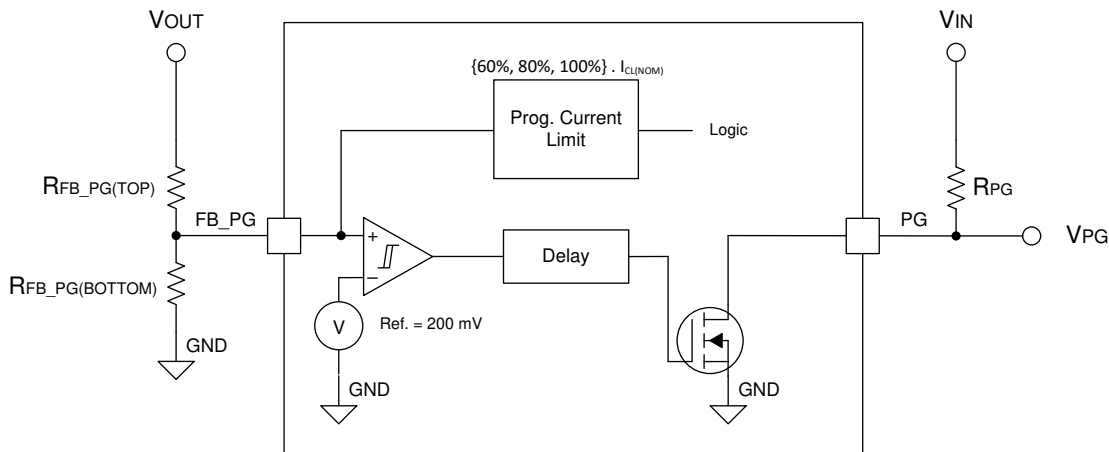


Figure 9-7. Programmable Power-Good Threshold Simplified Schematic

The PG pin pullup resistor value must be between 10 k Ω and 100 k Ω . The lower limit of 10 k Ω results from the maximum pulldown strength of the power-good transistor, and the upper limit of 100 k Ω results from the maximum leakage current at the power-good node. If the pullup resistor is outside of this range, then the power-good signal may not read a valid digital logic level.

The state of the PG signal is only valid when the FB_PG pin resistor divider network is set properly and the device is in normal operating mode.

9.1.7 Programmable Soft-Start and Noise-Reduction (NR/SS Pin)

The device features a programmable, monotonic, voltage-controlled, soft-start circuit that is set to work with an external capacitor ($C_{NR/SS}$). In addition to the soft-start feature, the $C_{NR/SS}$ capacitor also lowers the output voltage noise of the LDO. The soft-start feature can be used to eliminate power-up initialization problems. The controlled output voltage ramp also reduces peak inrush current during start up, minimizing start-up transients to the input power bus.

To achieve a monotonic start up, the device output voltage tracks the $V_{NR/SS}$ reference voltage until this reference reaches its set value (the set output voltage). The $V_{NR/SS}$ reference voltage is set by the $R_{NR/SS}$ resistor and, during start up, the device uses a fast charging current (I_{FAST_SS}) in addition to the $I_{NR/SS}$ current as shown in [Figure 9-8](#) to charge the $C_{NR/SS}$ capacitor.

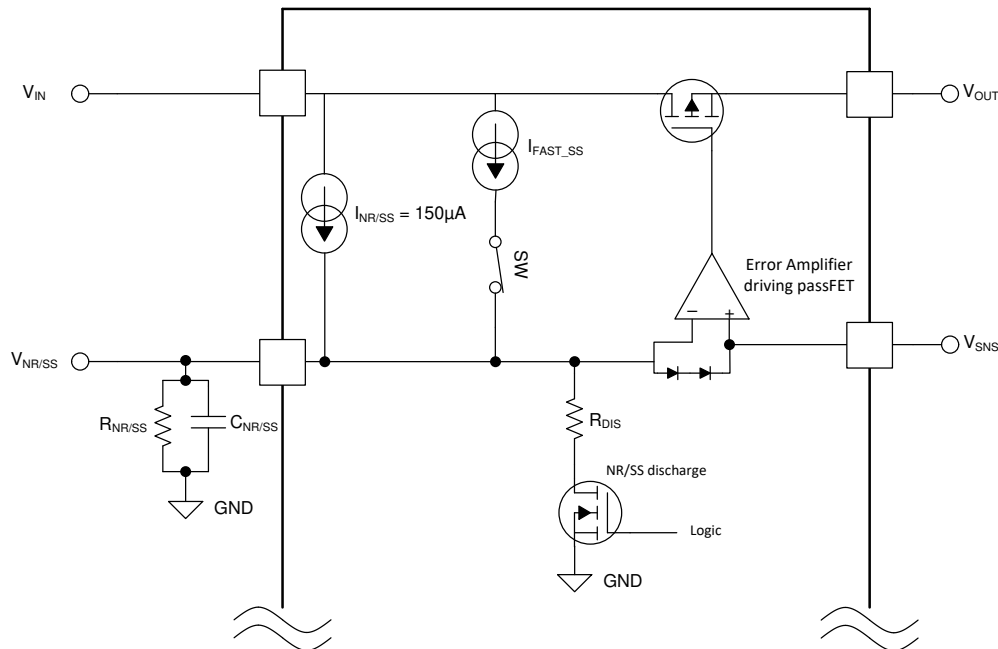


Figure 9-8. Simplified Soft-Start Circuit

The 2-mA (typical) I_{FAST_SS} current and 150 μ A (typical) $I_{NR/SS}$ current quickly charge $C_{NR/SS}$ until its voltage reaches approximately 93% of the set output voltage, then the I_{FAST_SS} current disengages and only the $I_{NR/SS}$ current continues to charge $C_{NR/SS}$ to its set output voltage level. If there is any error during start up or the output overshoot prevention circuit is triggered, the NR/SS discharge FET turns on, thus discharging the $C_{NR/SS}$ capacitor to protect both the LDO and the load.

The soft-start ramp time depends on the fast start-up (I_{FAST_SS}) charging current, the reference current ($I_{NR/SS}$), $C_{NR/SS}$ capacitor value, and the set (targeted) output voltage ($V_{OUT(target)}$). [Equation 4](#) calculates the soft-start ramp time.

$$\text{Soft-start time } (t_{SS}) = (V_{OUT(target)} \times C_{NR/SS}) / (I_{NR/SS} + I_{FAST_SS}) \quad (4)$$

The $I_{NR/SS}$ current is provided in the [Recommended Operating Conditions](#) table and has a value of 150 μ A (typical). The I_{FAST_SS} current has a value of 2 mA (typical) for $V_{IN} > 2.5$ V. [Figure 9-9](#) depicts the $I_{NR/SS}$ current versus V_{IN} and temperature.

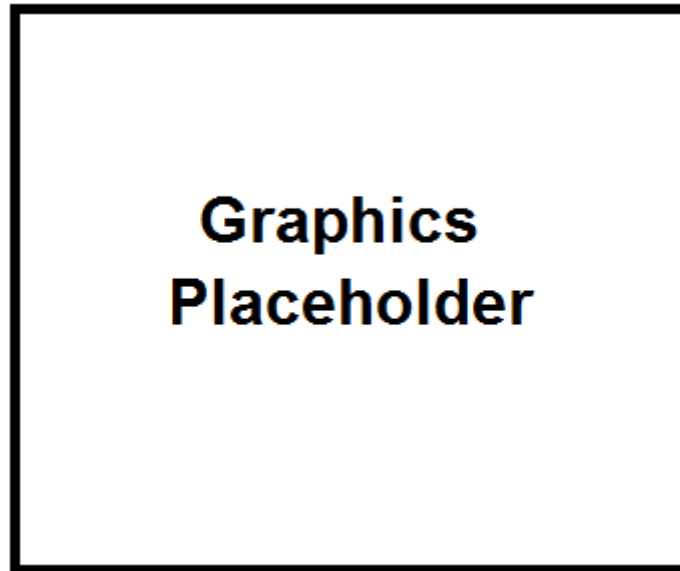


Figure 9-9. $I_{NR/SS}$ Current vs Input Supply and Temperature

Output voltage noise can be lowered significantly by increasing the $C_{NR/SS}$ capacitor. The $C_{NR/SS}$ capacitor and $R_{NR/SS}$ resistor form a low-pass filter (LPF) that filters out the noise from the $V_{NR/SS}$ voltage reference before being gained up with the error amplifier, thereby reducing the device noise floor. The LPF is a single-pole filter and Equation 5 calculates the LPF cutoff frequency. Increasing the $C_{NR/SS}$ capacitor can significantly lower output voltage noise, however, doing so greatly lengthens start-up time. For low-noise applications, use a 4.7- μ F $C_{NR/SS}$ for optimal noise and start-up time trade off.

$$\text{Cutoff Frequency (f}_{\text{cutoff}}) = 1 / (2 \times \pi \times R_{NR/SS} \times C_{NR/SS}) \quad (5)$$

The [Typical Characteristics](#) section illustrates the impact of the $C_{NR/SS}$ capacitor on the LDO output voltage noise.

9.1.8 Inrush Current

Inrush current is defined as the current into the LDO at the IN pin during start up. Inrush current then consists primarily of the sum of load current and the current used to charge the output capacitor. This current is difficult to measure because the input capacitor must be removed, which is not allowed for this device because the input capacitor is required for stability. However, Equation 6 can be used to estimate this current.

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT(t)}}{dt} \right] + \left[\frac{V_{OUT(t)}}{R_{LOAD}} \right] \quad (6)$$

where:

- $V_{OUT(t)}$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT(t)} / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

As shown in [Figure 9-8](#), the external capacitor at the NR/SS pin ($C_{NR/SS}$) sets the output start-up time by setting the rise time of the $V_{NR/SS}$ reference voltage.

9.1.9 Optimizing Noise and PSRR

Noise can be generally defined as any unwanted signal combining with the desired signal (such as the regulated LDO output) that results in a degraded power-supply source quality. Noise can easily be noticed in audio as a hissing or popping sound. Extrinsic and intrinsic are the two basic groups that noise can be categorized into. Noise produced from an external circuit or natural phenomena such as 50 to 60 hertz power-line noise (spikes), along with its harmonics, is an excellent representative of extrinsic noise. Intrinsic noise is produced by components within the device circuitry such as resistors and transistors. For this device, the two dominating sources of intrinsic noise are the error amplifier and the internal reference voltage ($V_{NR/SS}$). Another term that sometimes combines with extrinsic noise is PSRR, which refers to ability of the circuit or device to reject or filter-out input supply noise and is expressed as a ratio of output voltage noise, ripple to input voltage noise, or ripple.

Optimize the device intrinsic noise and PSRR by carefully selecting:

- $C_{NR/SS}$ for the low-frequency range up to the device bandwidth
- C_{OUT} for the high-frequency range close to and higher than the device bandwidth
- Operating headroom, $V_{IN} - V_{OUT}$ (V_{DO}), mainly for the low-frequency range up to the device bandwidth, but also for higher frequencies to a less effect

The device noise performance can be significantly improved by using a larger $C_{NR/SS}$ capacitor to filter out noise coupling from the input into the device $V_{NR/SS}$ reference. This coupling is especially apparent from low frequencies up to the device bandwidth. The low-pass filter formed by $C_{NR/SS}$ and $R_{NR/SS}$ can be designed to target low-frequency noise originating in the input supply. One downside of a larger $C_{NR/SS}$ capacitor is a longer start-up time. The device unity-gain configuration eliminates the noise performance degradation that other LDOs suffer from resulting from their feedback network. Furthermore, increasing the device load current has little to no effect on the device noise performance.

Further improvement to the device noise at a higher frequency range than the device bandwidth can be achieved by using a larger C_{OUT} capacitor. However, a larger C_{OUT} increases inrush current and slows down the device transient response.

Increasing the operational headroom between V_{IN} and V_{OUT} has little to no effect on improving noise performance. However, this increase does improve PSRR significantly for frequency ranges up to the device bandwidth. Higher headroom can also improve transient performance of the device as well. Although C_{OUT} has little to no effect on improving PSRR at low frequency, C_{OUT} can improve PSRR for higher frequencies beyond the device bandwidth. A larger C_{OUT} can also lengthen start-up time and increase start-up inrush current.

Table 9-2 lists the measured 10-Hz to 100-kHz RMS noise for a 3.3-V device output voltage with a 0.5-V headroom for different $C_{NR/SS}$ and C_{OUT} capacitors and a 1-A load current.

Table 9-2. Output Noise for 3.3- V_{OUT} vs $C_{NR/SS}$, C_{OUT} , and Typical Start-Up Time

V_n (μV_{RMS}), 10-Hz to 100-kHz BW	$C_{NR/SS}$ (μF)	C_{OUT} (μF)	START-UP TIME (ms)
1.0	0.47	10	3.62
0.98	1	10	3.73
0.62	2.2	10	6.21
0.46	4.7	10	13.97
0.42	10	10	28.21

9.1.10 Adjustable Operation

As shown in Figure 9-10, the output voltage of the device can be set using a single external resistor ($R_{NR/SS}$).

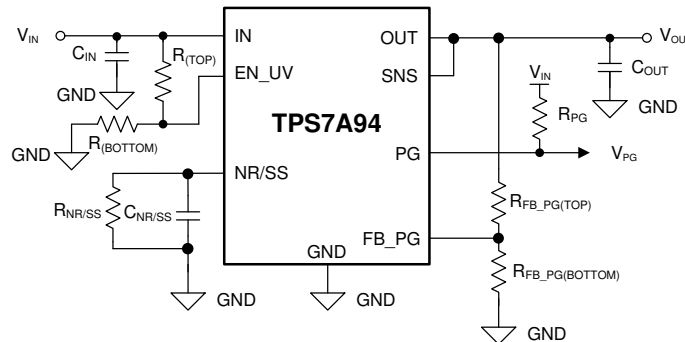


Figure 9-10. Typical Circuit

Use Equation 7 to calculate the $R_{NR/SS}$ value needed for the desirable output voltage.

$$V_{OUT} = I_{NR/SS(NOM)} \times R_{NR/SS} \quad (7)$$

Table 9-3 shows the recommended $R_{NR/SS}$ resistor values to achieve several common rails using a standard 0.5%-tolerance resistor.

Table 9-3. Recommended $R_{NR/SS}$ Values

TARGETED OUTPUT VOLTAGE (V)	$R_{NR/SS}$ (k Ω) ⁽¹⁾	CALCULATED OUTPUT VOLTAGE (V)
0.4	2.67	0.4005
0.5	3.32	0.498
0.6	4.02	0.603
0.7	4.64	0.696
0.8	5.36	0.804
0.9	6.04	0.906
1.0	6.65	0.9975
1.2	8.06	1.209
1.5	10.0	1.5
2.5	16.5	2.475
3.0	20.0	3.0
3.3	22.1	3.315
3.6	24.0	3.6
4.7	31.2	4.68
5.0	33.2	4.98

(1) 0.5% resistors.

9.1.11 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) and low equivalent series inductance (ESL) ceramic capacitors at the input, output, and noise-reduction pin. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature. The use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. Make sure to derate ceramic capacitors by at least 50%. The input and output capacitors

recommended herein account for a capacitance derating of approximately 50%, but at high V_{IN} and V_{OUT} conditions ($V_{IN} = 5.5\text{ V}$ to $V_{OUT} = 5.0\text{ V}$), the derating can be greater than 50%, and must be taken into consideration.

The device requires input, output, and noise-reduction capacitors for proper operation of the LDO. Use the nominal or larger than the nominal input, and output capacitors as specified in the [Recommended Operating Conditions](#) table. Place input and output capacitors as close as possible to corresponding pin and make the capacitor GND connections as close as possible to the device GND pin to shorten transient currents on the return path. Using a larger input capacitor or a bank of capacitors with various values is always good design practice to counteract input trace inductance, improve transient response, and reduce input ripple and noise. Using a larger output capacitor can also improve the transient response of the device..

Use the nominal noise reduction $C_{NR/SS}$ capacitor because using a larger $C_{NR/SS}$ capacitor can lengthen the start-up time as mentioned previously.

9.1.12 Load Transient Response

The load-step transient response is the LDO output voltage response to load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load, and the transition from a heavy to a light load. The regions shown in [Figure 9-11](#) are broken down in this section. Regions A, E, and H are where the output voltage is in steady-state regulation.

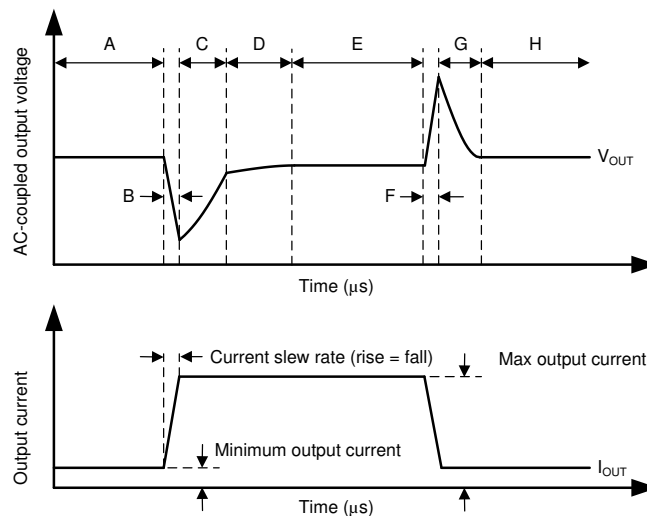


Figure 9-11. Load Transient Waveform

During transitions from a light load to a heavy load:

- The initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load:

- The initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor (region G)

Transitions between current levels changes the internal power dissipation because the device is a high-current device (region D). The change in power dissipation changes the die temperature during these transitions, and leads to a slightly different voltage level. This temperature-dependent output voltage level shows up in the various load transient responses.

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

9.1.13 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 8 calculates P_D :

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \quad (8)$$

Note

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The primary heat conduction path for the package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The power dissipation through the device determines the junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 9. The equation is rearranged for output current in Equation 10.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (9)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (10)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the [Electrical Characteristics](#) table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the DSC package junction-to-case (bottom) thermal resistance ($R_{\theta JCBot}$) plus the thermal resistance contribution by the PCB copper.

9.1.14 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 11 and are given in the [Electrical Characteristics](#) table.

$$\begin{aligned} \Psi_{JT}: T_J &= T_T + \Psi_{JT} \times P_D \\ \Psi_{JB}: T_J &= T_B + \Psi_{JB} \times P_D \end{aligned} \quad (11)$$

where:

- P_D is the power dissipated as explained in [Equation 8](#)
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

9.1.15 TPS7A94EVM-046 Thermal Analysis

The [TPS7A94EVM-046](#) was used to develop the TPS7A9401DRC thermal model. The DRC package is a 3-mm × 3-mm, 10-pin VQFN with 25-μm plating on each via. The EVM is a 2.85-inch × 3.35-inch (72.39 mm × 85.09 mm) PCB comprised of four layers. [Table 9-4](#) lists the layer stackup for the EVM. [Figure 9-12](#) to [Figure 9-16](#) illustrate the various layer details for the EVM.

Table 9-4. TPS7A94EVM-046 PCB Stackup

LAYER	NAME	MATERIAL	THICKNESS (mil)
1	Top overlay	—	—
2	Top solder	Solder resist	0.4
3	Top layer	Copper	2.8
4	Dielectric 1	FR-4 high Tg	10
5	Mid layer 1	Copper	2.8
6	Dielectric 2	FR-4 high Tg	30
7	Mid layer 2	Copper	2.8
8	Dielectric 3	FR-4 high Tg	10
9	Bottom layer	Copper	2.8
10	Bottom solder	Solder resist	0.4

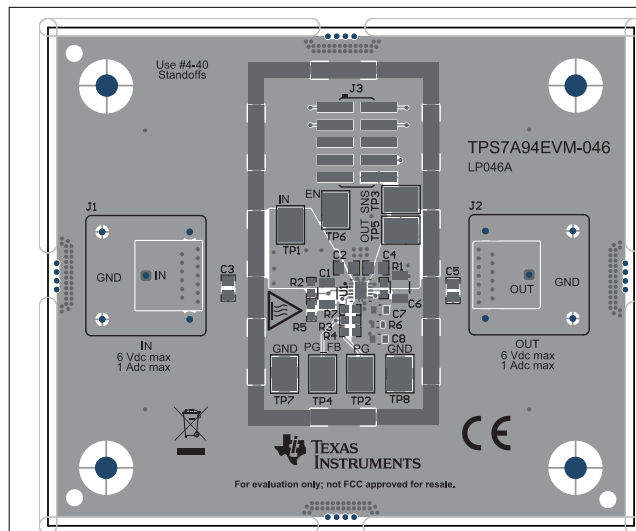


Figure 9-12. Top Composite View

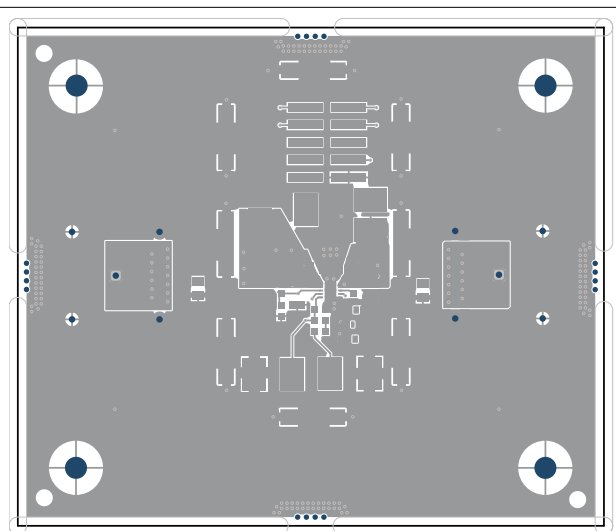


Figure 9-13. Top Layer Routing

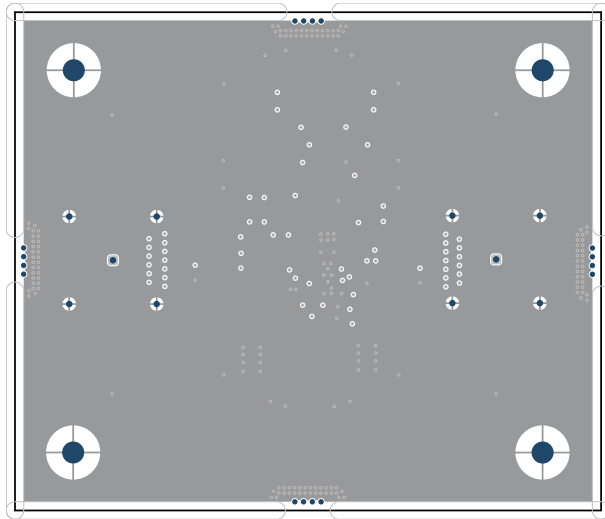


Figure 9-14. Mid Layer 1 Routing

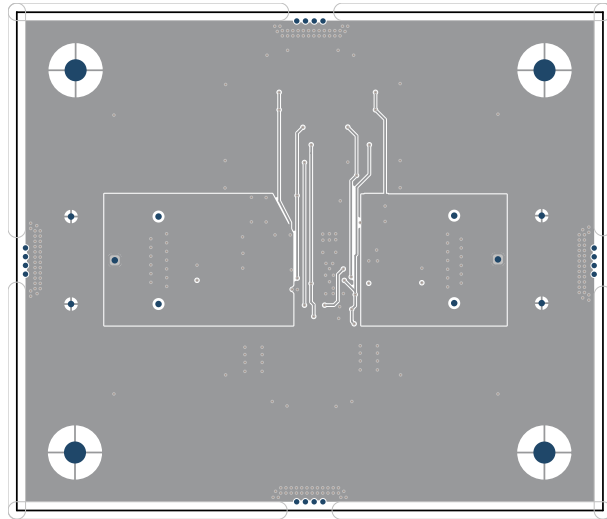


Figure 9-15. Mid Layer 2 Routing

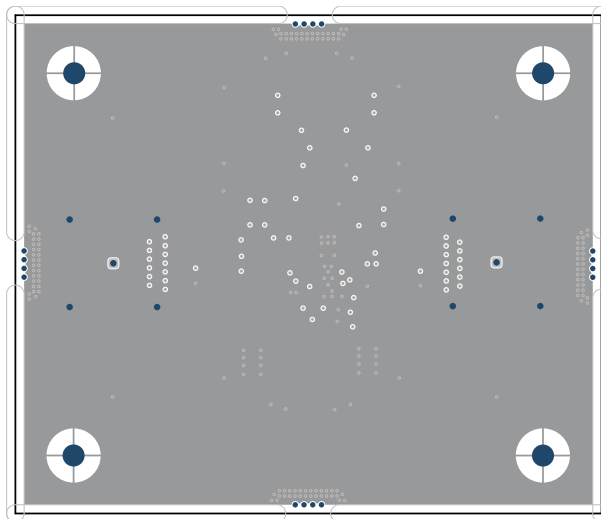


Figure 9-16. Bottom Layer Routing

TPS7A94

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Figure 9-17 to Figure 9-19 show the thermal gradient on the PCB and device that results when a 1-W power dissipation is used through the PassFET with a 25°C ambient temperature. Table 9-5 shows thermal simulation data for the TPS7A94EVM-046.

Table 9-5. TPS7A94EVM-046 Thermal Simulation Data

DUT	$R_{\theta JA}$ (°C/W)	ψ_{JB} (°C/W)	ψ_{JT} (°C/W)
TPS7A94EVM-046	25.6	11.5	0.3

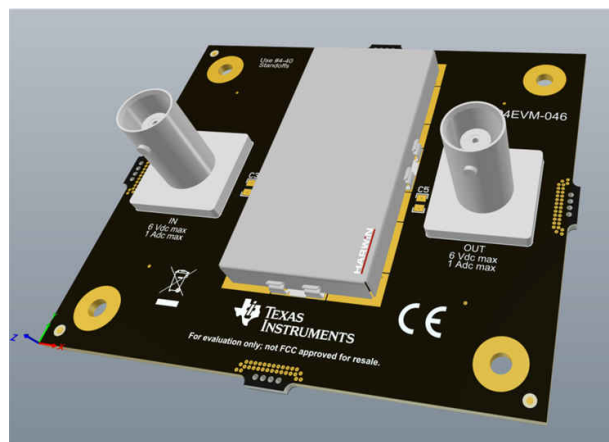


Figure 9-17. TPS7A94EVM-046 3D View

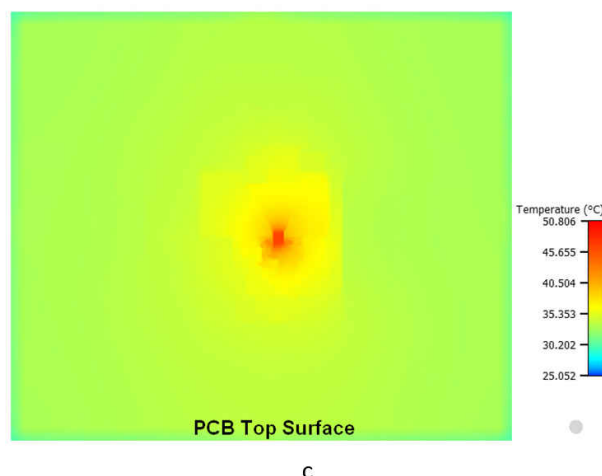


Figure 9-18. TPS7A94EVM-46 PCB Thermal Gradient

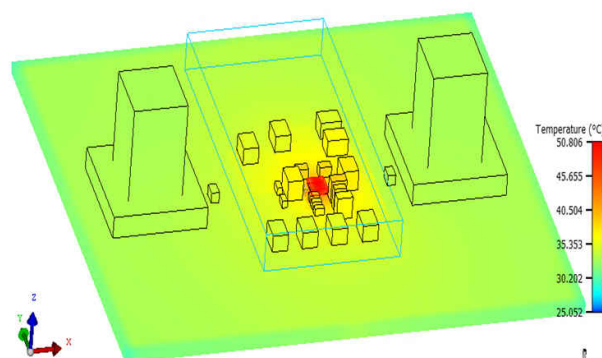


Figure 9-19. TPS7A94EVM-46 Device Thermal Gradient

9.2 Typical Application

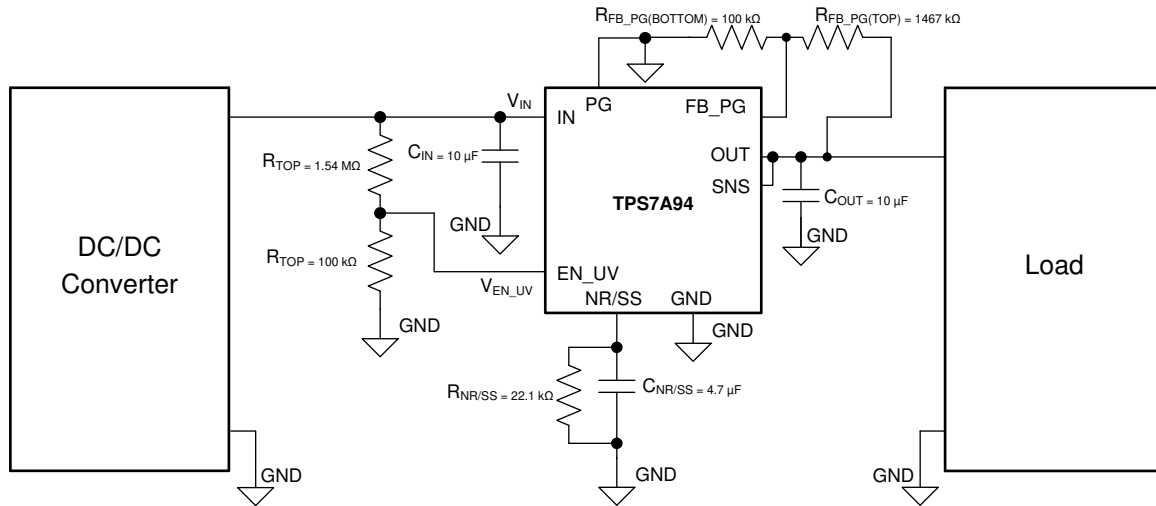


Figure 9-20. Typical Application Circuit

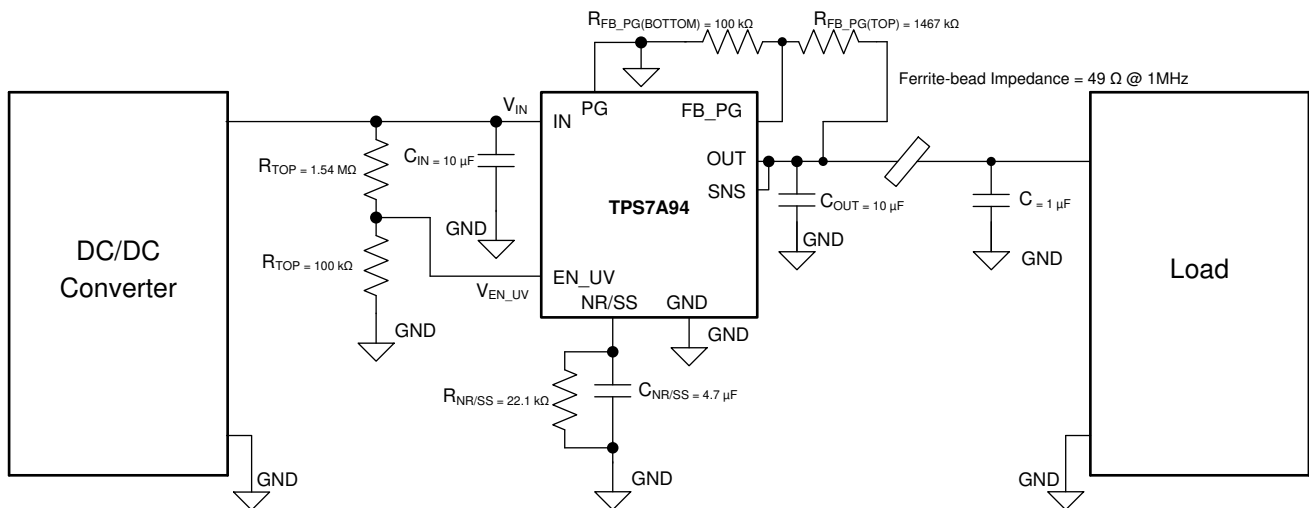


Figure 9-21. Typical Application Circuit With Added Pi-Filter

9.2.1 Design Requirements

Table 9-6 lists the required application parameters for this design example.

Table 9-6. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	$V_{IN} \geq 5\text{ V}$, $\pm 3\%$, provided by the dc/dc converter switching at 1 MHz
Output voltage	3.3 V, $\pm 1\%$
Output current	500 mA (maximum), 300 mA (minimum)
Current limit	750 mA
PG threshold	95%
Targeted spectral noise	Targeted noise compliance mask Zone 1 (10 Hz to 100 Hz): Spectral noise $\leq 100\text{ nV}/\sqrt{\text{Hz}}$ Zone 2 (100 Hz to 1 kHz): Spectral noise $\leq 10\text{ nV}/\sqrt{\text{Hz}}$ Zone 3 (> 1 kHz): Spectral noise $\leq 3\text{ nV}/\sqrt{\text{Hz}}$
PSRR at 1 MHz	> 50 dB at max load current
Start-up environment	Device to be enabled when $V_{IN} \geq 80\% \times V_{IN_Target}$ Device to be disabled when $V_{IN} < 80\% \times V_{IN_Target}$ Start-up time < 25 ms

9.2.2 Detailed Design Procedure

In this design example, the TPS7A94 is powered by a dc/dc convertor switching at 1 MHz. The load requires a 3.3-V clean rail with the spectral noise mask versus frequency shown in Figure 9-22 and a maximum load of 500 mA. The typical 10- μF input and output capacitors and 4.7- μF NR/SS capacitors are used to achieve a good balance between fast start-up time and excellent noise and PSRR performance.

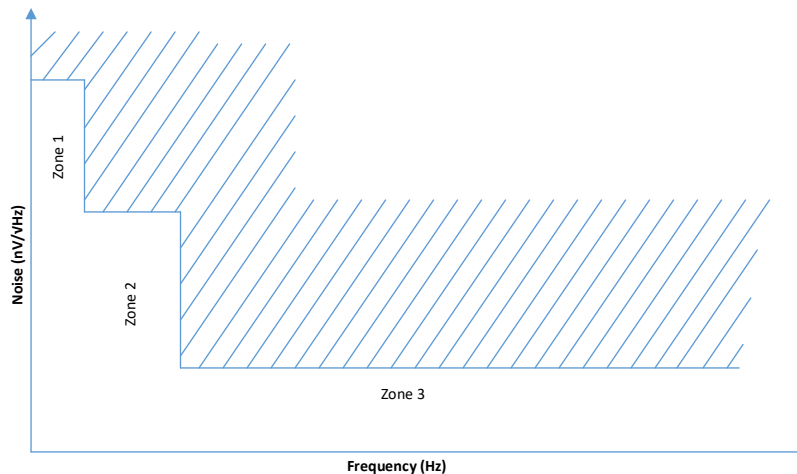


Figure 9-22. Noise Compliance Mask

The TPS7A94 output voltage is set using a 22.1-k Ω , thin-film resistor calculated using Equation 7. To set the current limit to a value close to the 750 mA required by the application, and to set the PG threshold to 95%, use Table 9-1 to set the R_{FB_PG} top and bottom resistors values at 1.47 M Ω and 100 k Ω , respectively.

To set the enable and disable voltages for the device, use the precision enable circuit to set the external UVLO voltage levels as follows: V_{OFF} must be < 80 % of V_{IN} , so set V_{OFF} to 3.75 V. V_{ON} is calculated using Equation 1 externally to be 4 V by choosing the bottom resistor value for the precision enable to be 100 k Ω , then using Equation 2 to calculate the top resistor to be 1.54 M Ω .

Figure 9-23 illustrates that the device meets all design noise requirements except for the noise peaking at 900 kHz. However, this noise peaking can easily be attenuated to the required noise level by means of a pi-filter positioned after the LDO. Figure 9-24 illustrates that this design is very close to the PSRR level at 1 MHz and

may require more margin. Fortunately, both requirements are easily achieved by inserting a pi-filter consisting of a ferrite bead and a small capacitor beyond the LDO and before the load; see [Figure 9-21](#).

The ferrite bead was selected to have a very small DC resistance of less than 50 mΩ, 1 A of current rating, and a relatively small footprint. The added pi-filter components have almost no impact on the LDO accuracy performance and no significant increase in the design total cost.

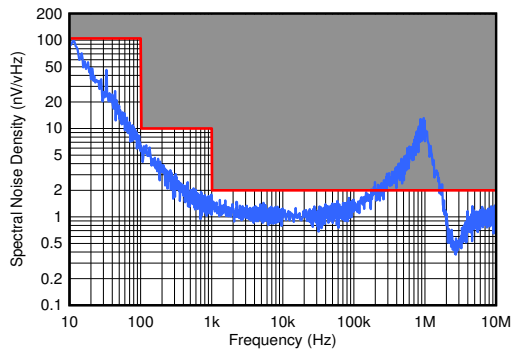


Figure 9-23. Output Noise vs Frequency

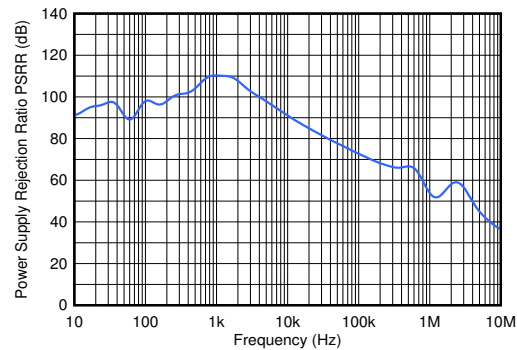


Figure 9-24. PSRR vs Frequency

9.2.3 Application Curves

[Figure 9-25](#) and [Figure 9-26](#) show the design noise and PSRR performance after inserting the pi-filter.

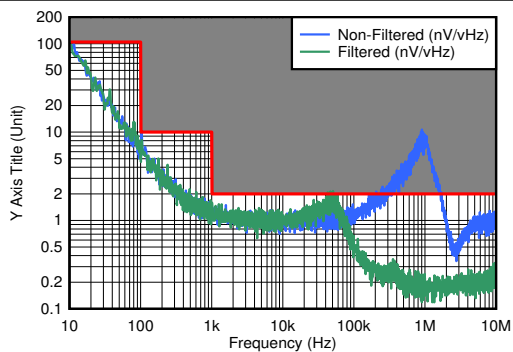


Figure 9-25. Noise vs Frequency

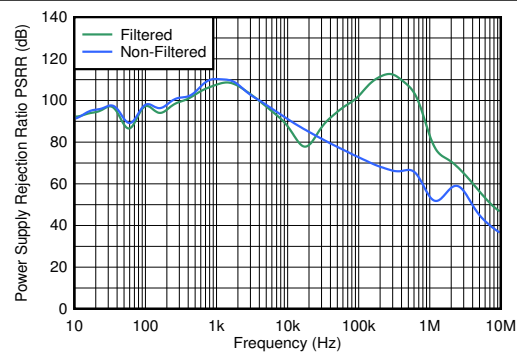


Figure 9-26. PSRR vs Frequency

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.7 V and 5.7 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, use additional input capacitors with low ESR to help improve output noise performance.

11 Layout

11.1 Layout Guidelines

11.1.1 Board Layout

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. To avoid negative system performance, do not use vias or long traces to the input and output capacitors. The grounding and layout scheme illustrated in [Figure 11-1](#) minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

To improve performance, use a ground reference plane, either embedded in the PCB itself or placed on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

11.1.2 Layout Example

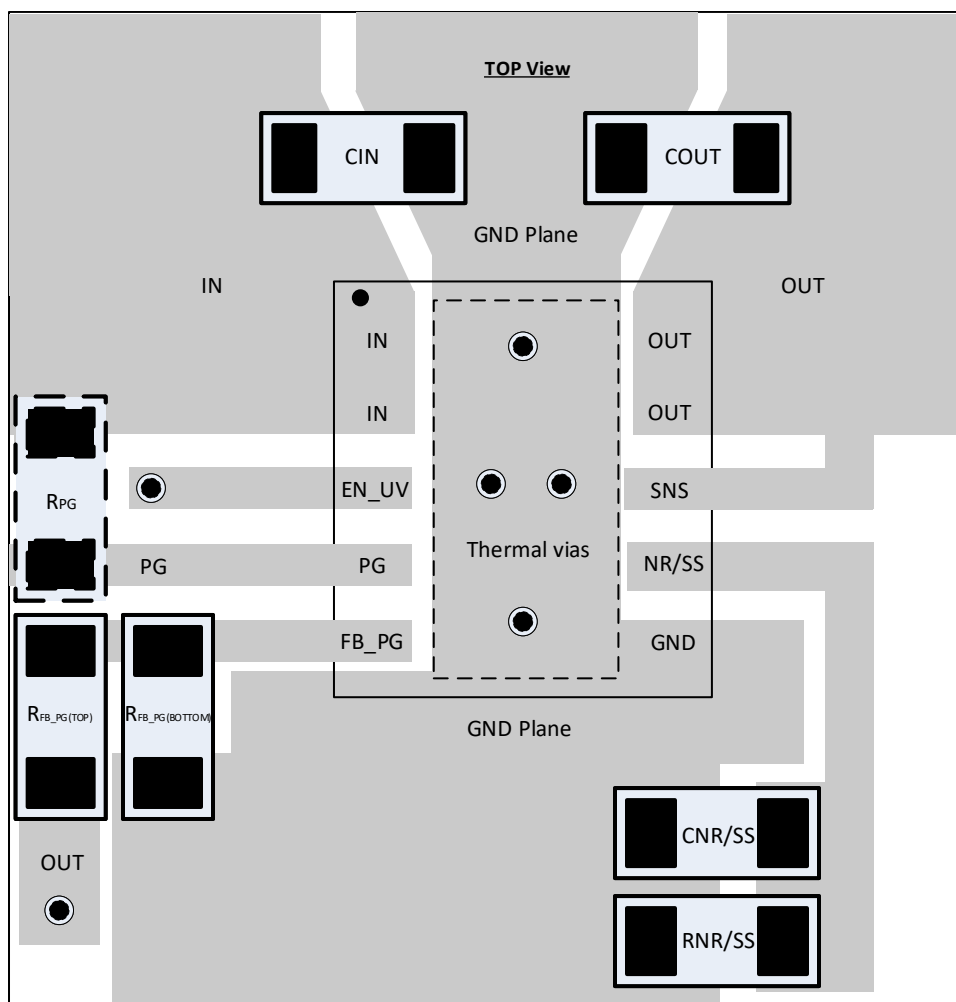


Figure 11-1. Example Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A94. [Table 12-1](#) shows the summary information for this fixture.

Table 12-1. Design Kits and Evaluation Modules

NAME	LITERATURE NUMBER
TPS7A94EVM-046 evaluation module	SBVU070

The EVM can be requested at the Texas Instruments [web site](#) through the TPS7A94 product folder.

12.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A94 is available through the TPS7A94 product folder under simulation models.

12.1.2 Device Nomenclature

Table 12-2. Ordering Information

PRODUCT	DESCRIPTION
TPS7A94 yyy z	yyy is the package designator. z is the package quantity.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [TPS3702 High-Accuracy, Overvoltage and Undervoltage Monitor data sheet](#)
- Texas Instruments, [TPS7A94EVM-046 Evaluation Module user guide](#)
- Texas Instruments, [Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator application report](#)
- Texas Instruments, [6 A Current-Sharing Dual LDO reference guide](#)
- Texas Instruments, [High-Current, Low-Noise Parallel LDO reference design](#)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

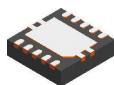
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

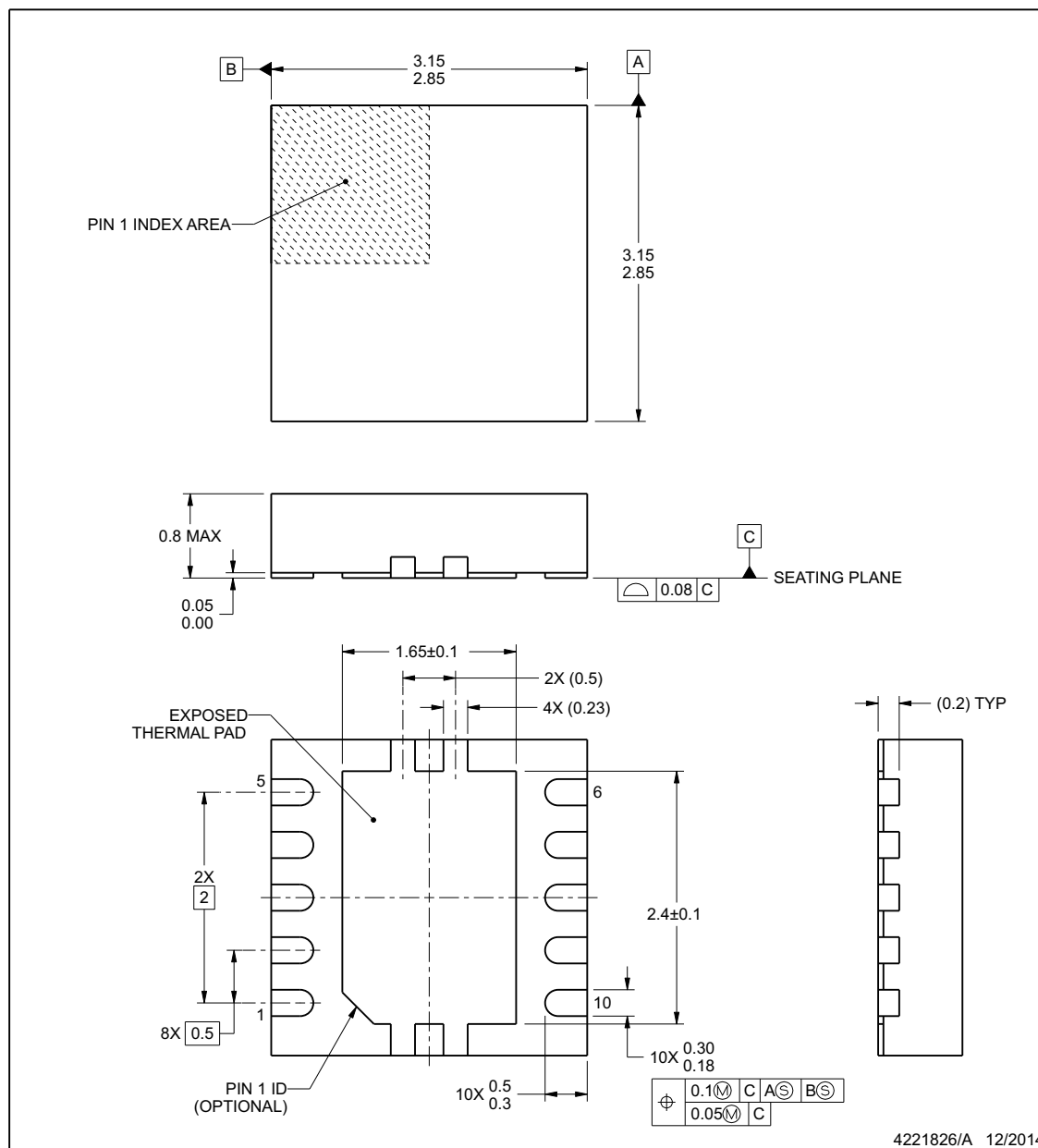


PACKAGE OUTLINE

DSC0010J

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



ADVANCE INFORMATION

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

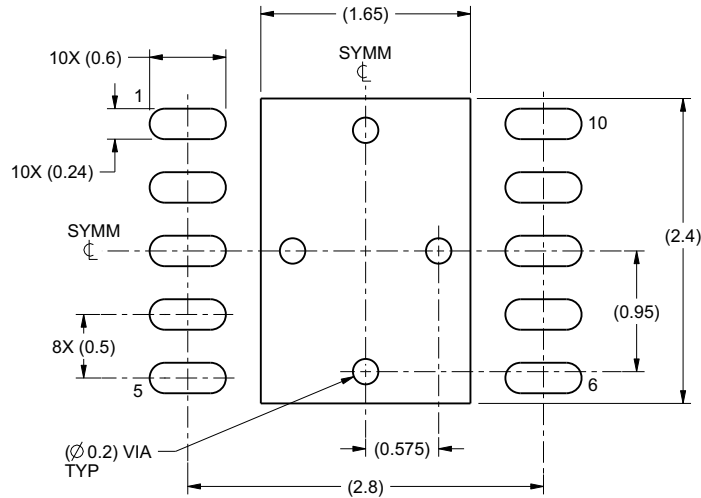
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EXAMPLE BOARD LAYOUT

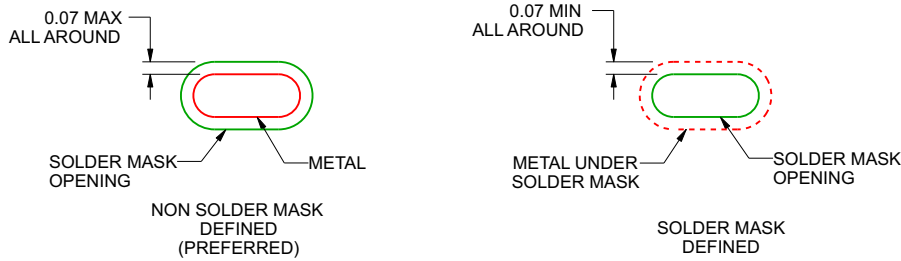
DSC0010J

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4221826/A 12/2014

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

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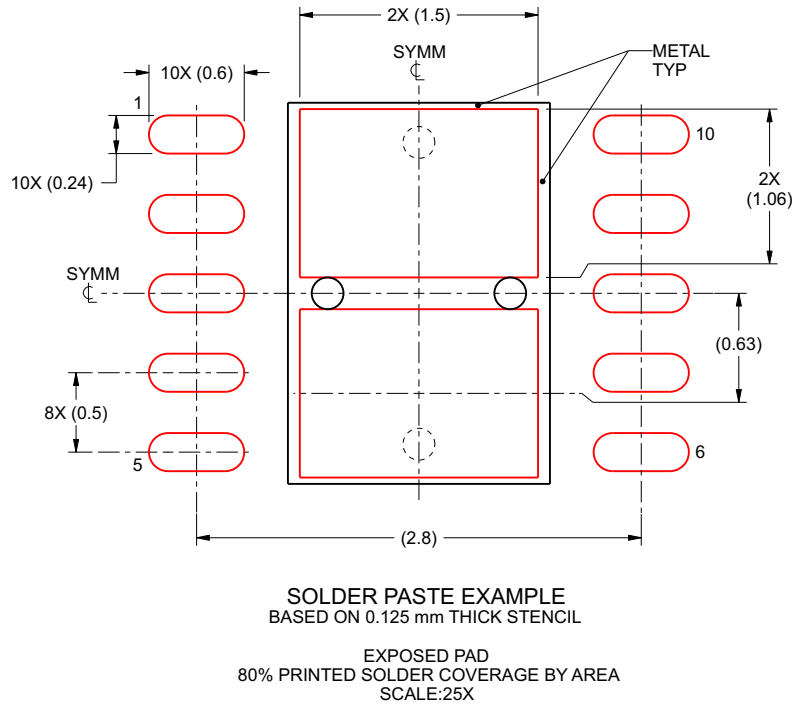
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DSC0010J

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4221826/A 12/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS7A9401DSCR	ACTIVE	WSO	DSC	10	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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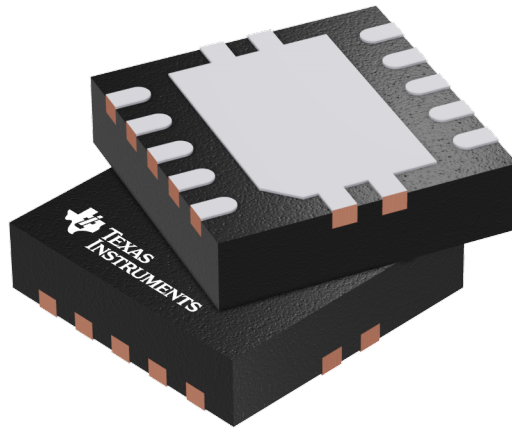
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

DSC 10

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207383/F

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