

# 具有 SMBus 和 I<sup>2</sup>C 兼容接口的 TMP116x 高精度、低功耗数字温度传感器

## 1 特性

- **TMP116 精度无需校准:**
  - $-10^{\circ}\text{C}$  至  $+85^{\circ}\text{C}$  范围内为  $\pm 0.2^{\circ}\text{C}$  (最大值)
  - $-40^{\circ}\text{C}$  至  $+105^{\circ}\text{C}$  范围内为  $\pm 0.25^{\circ}\text{C}$  (最大值)
  - $+105^{\circ}\text{C}$  至  $+125^{\circ}\text{C}$  范围内为  $\pm 0.3^{\circ}\text{C}$  (最大值)
- **TMP116 精度无需校准**
  - $-25^{\circ}\text{C}$  至  $+85^{\circ}\text{C}$  范围内为  $\pm 0.3^{\circ}\text{C}$  (最大值)
  - $-40^{\circ}\text{C}$  至  $+125^{\circ}\text{C}$  范围内为  $\pm 0.4^{\circ}\text{C}$  (最大值)
- **低静态电流:**
  - 3.5 $\mu\text{A}$ 、1Hz 转换周期
  - 250nA 关断电流
- **电源范围: 1.9V 至 5.5V**
- **分辨率: 0.0078 $^{\circ}\text{C}$  时为 16 位 (1LSB)**
- **可编程温度警报限值**
- **通用 EEPROM: 64 位**
- **NIST 可追溯性**
- **SMBus<sup>TM</sup>, I<sup>2</sup>C 接口兼容性**

## 2 应用

- 环境监控和恒温器
- 可穿戴设备
- 资产跟踪和冷藏链
- 燃气表和热量计
- 测试和测量
- RTD 更换: PT100、PT500、PT1000
- 热电偶冷端补偿

## 3 说明

TMP116 (TMP116、TMP116N) 是一系列具有集成 EEPROM 存储器的低功耗、高精度温度传感器。TMP116 可提供 16 位温度结果, 具有 0.0078 $^{\circ}\text{C}$  的分辨率, 且无需校准即可实现高达  $\pm 0.2^{\circ}\text{C}$  的精度。TMP116 可兼容 I<sup>2</sup>C 和 SMBus 接口, 具有可编程警报功能, 在单路总线上最多可支持 4 个器件。

TMP116 不仅节省功耗, 而且消耗最低电流, 能够最大限度减少自发热并提高测量精度。TMP116 在 1.9V 至 5.5V 电压范围内运行, 电流消耗通常为 3.5 $\mu\text{A}$ 。

TMP116 器件运行温度范围为  $-55^{\circ}\text{C}$  至  $+125^{\circ}\text{C}$ , 精度比 A 类 RTD 要高, 但电流消耗不足 PT100 RTD 典型激励电流的五分之一。相比于 RTD, TMP116 更易于使用, 无需校准、外部电路、匹配的线迹和开尔文连接。

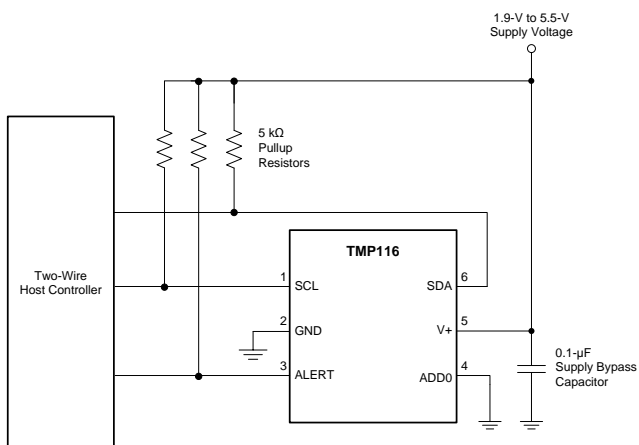
TMP116 装置在生产调试阶段经完全测试, 可通过 NIST 进行追溯, 且使用经 ISO/IEC 17025 认证标准校准的设备进行了验证。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TMP116	WSON (6)	2.00mm x 2.00mm

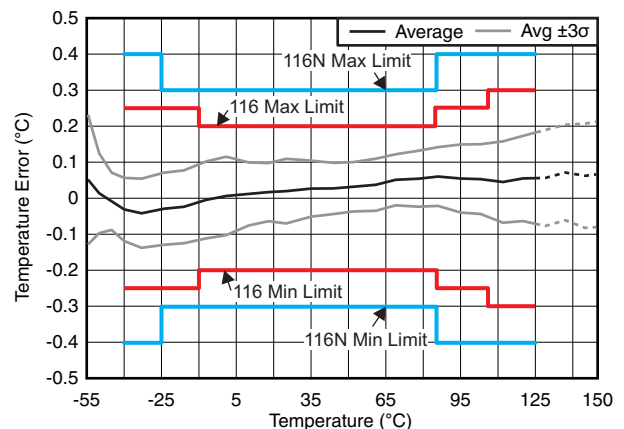
(1) 要了解所有可用封装, 请见数据表末尾的封装选项附录。

简化电路原理图



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温度精度



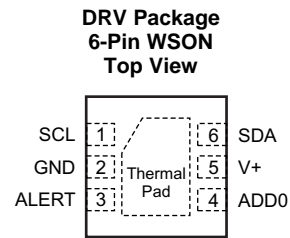
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## 4 修订历史记录

日期	修订版本	注释
2017 年 5 月	*	首次发布。

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SCL	I	Serial clock
2	GND	—	Ground
3	ALERT	O	Overtemperature alert or data-ready signal. Open-drain output; requires a pullup resistor.
4	ADD0	I	Address select. Connect to GND, V+, SDA, or SCL.
5	V+	I	Supply voltage, 1.9 V to 5.5 V
6	SDA	I/O	Serial data. Open-drain output; requires a pullup resistor.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
Supply voltage, V+	-0.3	6	V
Voltage at SCL, SDA, ALERT, and ADD0	-0.3	6	V
Operating junction temperature, T <sub>J</sub>	-55	150	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V+	Supply voltage	1.9	3.3	5.5	V
T <sub>A</sub>	Operating free-air temperature	-55		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TMP116	UNIT
		DRV (WSON)	
		6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	68.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	70.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	9.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	38.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.7	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	38.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

minimum and maximum specifications are over  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and  $V_{+} = 1.9\text{ V}$  to  $5.5\text{ V}$  (unless otherwise noted); typical specifications are at  $T_{A} = 25^{\circ}\text{C}$  and  $V_{+} = 3.3\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TEMPERATURE-TO-DIGITAL CONVERTER</b>						
Temperature accuracy <sup>(1)</sup>	TMP116	$-10^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , $V_{+} = 3.3\text{ V}$	-0.2	$\pm 0.1$	0.2	$^{\circ}\text{C}$
		$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$ , $V_{+} = 3.0\text{ V}$ to $3.6\text{ V}$	-0.25	$\pm 0.2$	0.25	
		$+105^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ , $V_{+} = 3.0\text{ V}$ to $3.6\text{ V}$	-0.3	$\pm 0.25$	0.3	
		$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ , $V_{+} = 1.9\text{ V}$ to $5.5\text{ V}$ <sup>(2)</sup>	-0.4	$\pm 0.3$	0.4	
	TMP116N	$-25^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , $V_{+} = 3.3\text{ V}$	-0.3	$\pm 0.2$	0.3	
		$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ , $V_{+} = 3.0\text{ V}$ to $3.6\text{ V}$	-0.4	$\pm 0.3$	0.4	
		$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ , $V_{+} = 1.9\text{ V}$ to $5.5\text{ V}$ <sup>(2)</sup>	-0.5	$\pm 0.4$	0.5	
DC power-supply sensitivity	One-shot mode, 8 averages, $T_{A} = 25^{\circ}\text{C}$	0	20	55	$\text{m}^{\circ}\text{C}/\text{V}$	
Temperature resolution (LSB)			7.8125		$\text{m}^{\circ}\text{C}$	
Repeatability <sup>(3)</sup>	$V_{+} = 3.3\text{ V}$ , 8 averages, 1-Hz sampling		$\pm 1$		LSB	
Long-term stability and drift	300 hours at $150^{\circ}\text{C}$ <sup>(4)</sup>		$\pm 0.05$		$^{\circ}\text{C}$	
Temperature cycling and hysteresis <sup>(5)</sup>	8 averages		$\pm 1$		LSB	
<b>DIGITAL INPUT/OUTPUT</b>						
Input capacitance			3		pF	
$V_{IH}$	Input logic high level		0.7 ( $V_{+}$ )		V	
$V_{IL}$	Input logic low level			0.3 ( $V_{+}$ )	V	
$I_{IN}$	Input current		-0.2		$\mu\text{A}$	
$V_{OLS}$	SDA output logic low level	$I_{OL} = -3\text{ mA}$	0		0.4	V
$V_{OLA}$	$\overline{\text{ALERT}}$ output logic low level	$I_{OL} = -3\text{ mA}$	0		0.4	V
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent current	Active conversion, serial bus inactive		135	220	$\mu\text{A}$
		1-Hz conversion cycle, averaging mode off, serial bus inactive, $25^{\circ}\text{C}$		3.5	4.5	
		1-Hz conversion cycle, 8 averages mode, serial bus inactive, $25^{\circ}\text{C}$		16	22	
		1-Hz conversion cycle, averaging mode off, serial bus active, SCL frequency = 400 kHz		21		
$I_{SB}$	Standby current <sup>(6)</sup>	Serial bus inactive, SCL and SDA = $V_{+}$ , $25^{\circ}\text{C}$		1.25	2.1	$\mu\text{A}$
$I_{SD}$	Shutdown current	Serial bus inactive, SCL and SDA = $V_{+}$ , $25^{\circ}\text{C}$		0.25	0.5	$\mu\text{A}$
		Serial bus inactive, SCL and SDA = $V_{+}$ , $125^{\circ}\text{C}$			8.5	
		Serial bus active, SCL frequency = 400 kHz		17		
$I_{EE}$	EEPROM write quiescent current	ADC conversion off; serial bus inactive		240		$\mu\text{A}$
$V_{POR}$	Power-on-reset threshold voltage	$V_{+}$ rising		1.6		V
	Brownout detect	$V_{+}$ falling		1.1		V
	Reset time	Time required by device to reset		1.5		ms
	Active conversion time	1 conversion	13.5	15.5	17	ms

(1) 8 averages, 1-Hz conversion cycle.

(2)  $\pm 0.75^{\circ}\text{C}$  maximum error between  $-55^{\circ}\text{C}$  to  $-40^{\circ}\text{C}$ .

(3) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.

(4) Long-term stability is determined using accelerated operational life testing at a junction temperature of  $150^{\circ}\text{C}$ .

(5) Hysteresis is defined as the ability to reproduce a temperature reading as the temperature varies from room  $\rightarrow$  hot  $\rightarrow$  room  $\rightarrow$  cold  $\rightarrow$  room. The temperatures used for this test are  $-40^{\circ}\text{C}$ ,  $25^{\circ}\text{C}$ , and  $125^{\circ}\text{C}$ .

(6) Quiescent current between conversions.

## Electrical Characteristics (continued)

minimum and maximum specifications are over  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and  $V+ = 1.9\text{ V}$  to  $5.5\text{ V}$  (unless otherwise noted); typical specifications are at  $T_A = 25^{\circ}\text{C}$  and  $V+ = 3.3\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>EEPROM</b>					
Programming time			7		ms
Number of writes		1,000	50,000		Times
Data retention time		10	100		Years

### 6.6 Two-Wire Interface Timing

minimum and maximum specifications are over  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $V+ = 1.9\text{ V}$  to  $5.5\text{ V}$  (unless otherwise noted); typical specifications are at  $T_A = 25^{\circ}\text{C}$  and  $V+ = 3.3\text{ V}$ ; values are based on statistical analysis of samples tested during initial release

		MIN	MAX	UNIT
$f_{\text{SCL}}$	SCL operating frequency	1	400	kHz
$t_{\text{BUF}}$	Bus free time between STOP and START conditions	1300		ns
$t_{\text{HD;STA}}$	Hold time after repeated START condition. After this period, the first clock is generated.	600		ns
$t_{\text{SU;STA}}$	Repeated START condition setup time	600		ns
$t_{\text{SU;STO}}$	STOP condition setup time	600		ns
$t_{\text{HD;DAT}}$	Data hold time	0		ns
$t_{\text{VD;DAT}}$	Data valid time <sup>(1)</sup>		0.9	$\mu\text{s}$
$t_{\text{SU;DAT}}$	Data setup time	100		ns
$t_{\text{LOW}}$	SCL clock low period	1300		ns
$t_{\text{HIGH}}$	SCL clock high period	600		ns
$t_{\text{F}} - \text{SDA}$	Data fall time	$20 \times (V+ / 5.5)$	300	ns
$t_{\text{F}}, t_{\text{R}} - \text{SCL}$	Clock fall and rise time		300	ns
$t_{\text{R}}$	Rise time for SCL $\leq 100\text{ kHz}$		1000	ns
	Serial bus timeout (SDA bus released if there is no clock)	20	40	ms

(1)  $t_{\text{VD;DATA}}$  = time for data signal from SCL low to SDA output (high to low, depending on which is worse).

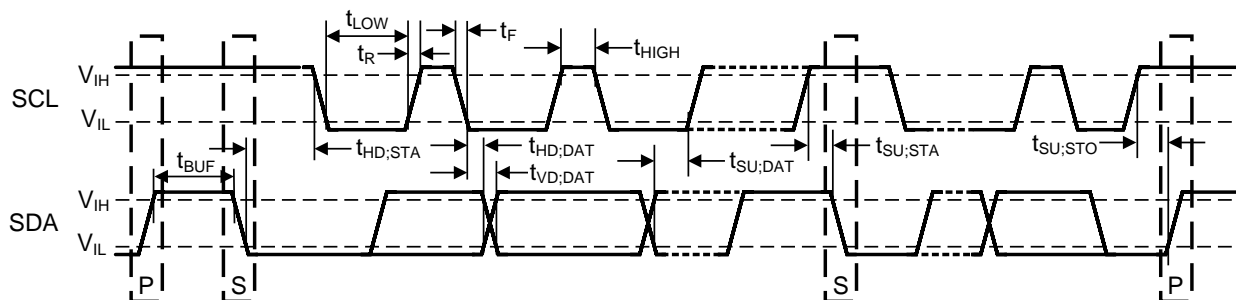
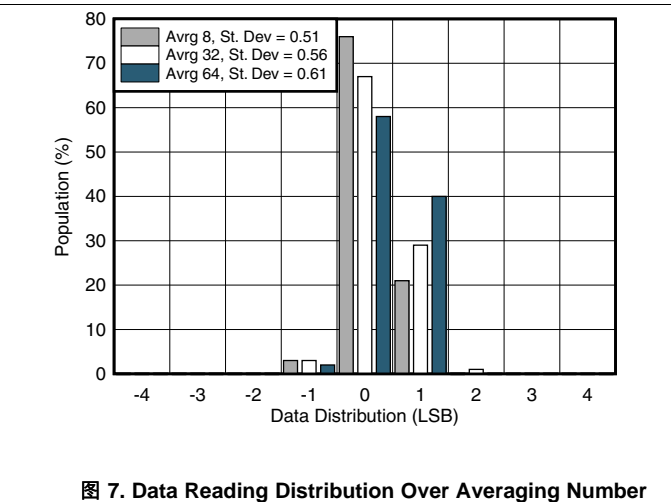
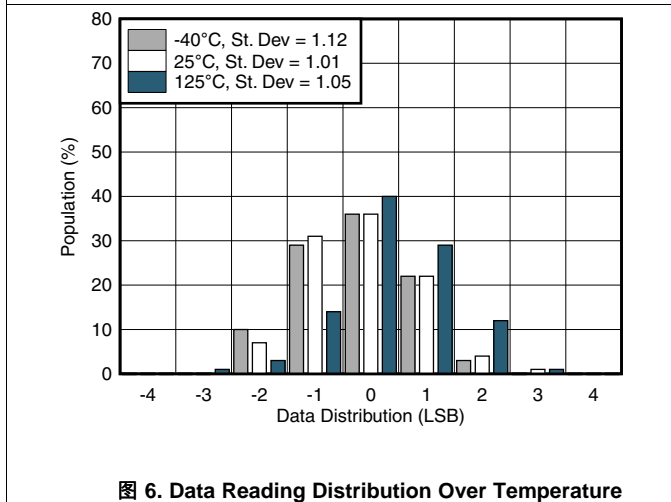
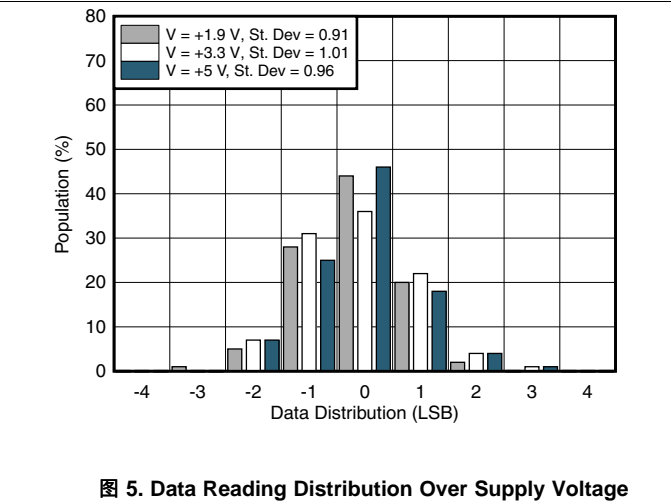
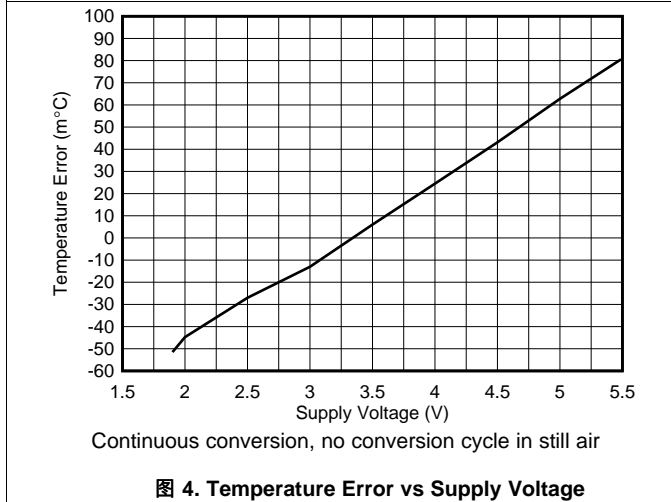
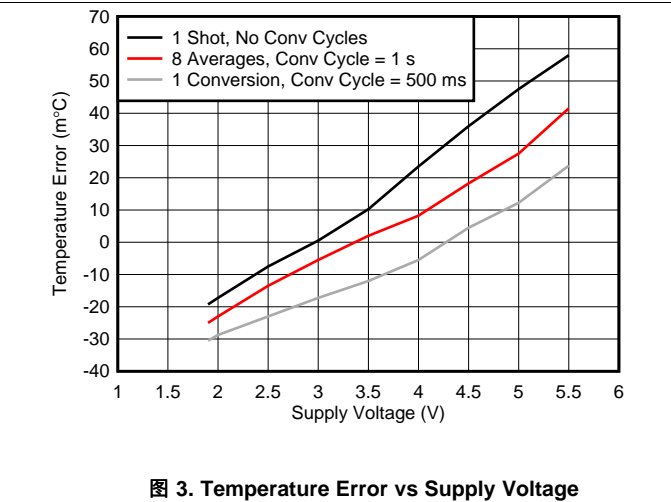
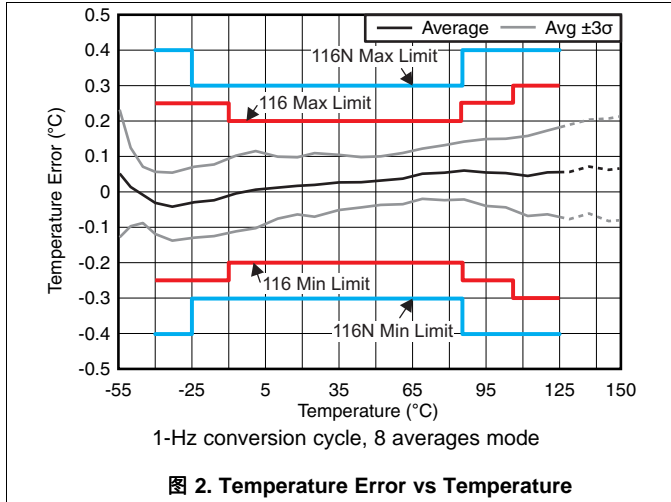


图 1. Two-Wire Timing Diagram

### 6.7 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_+ = 3.3\text{ V}$ , and measurement taken in oil bath (unless otherwise noted)



Typical Characteristics (接下页)

at  $T_A = 25^\circ\text{C}$ ,  $V_+ = 3.3\text{ V}$ , and measurement taken in oil bath (unless otherwise noted)

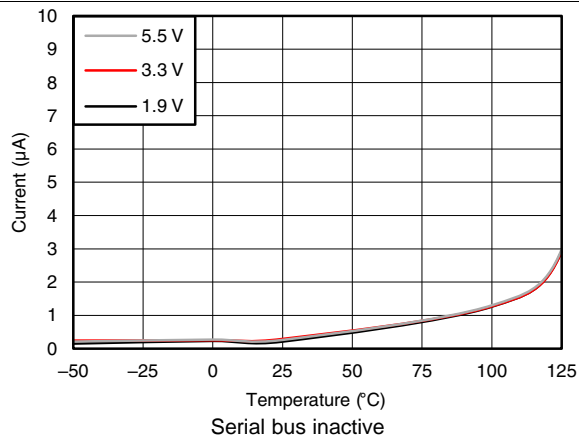


图 8. Quiescent Current in Shutdown Mode

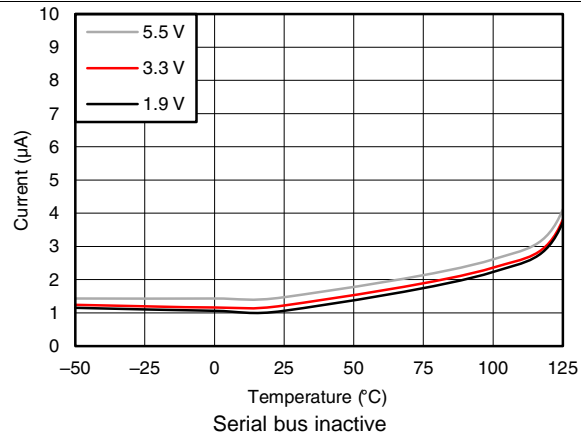


图 9. Quiescent Current in Standby Mode

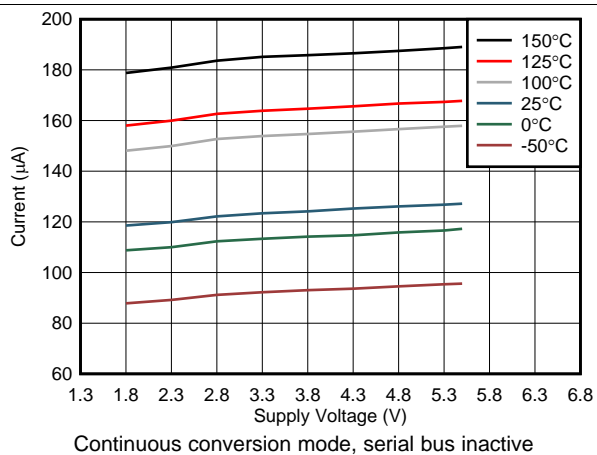


图 10. Quiescent Current During Active Conversion

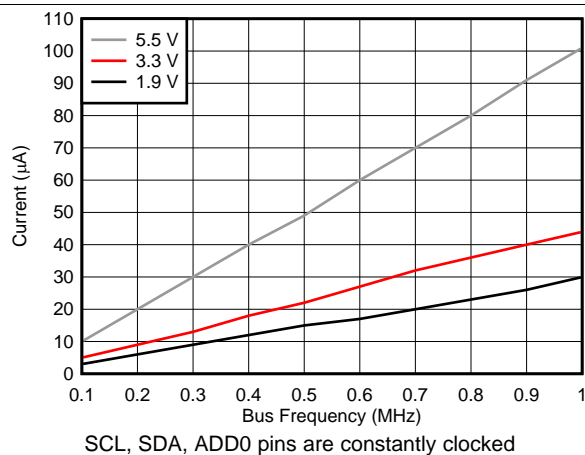


图 11. Quiescent Current in Shutdown Mode

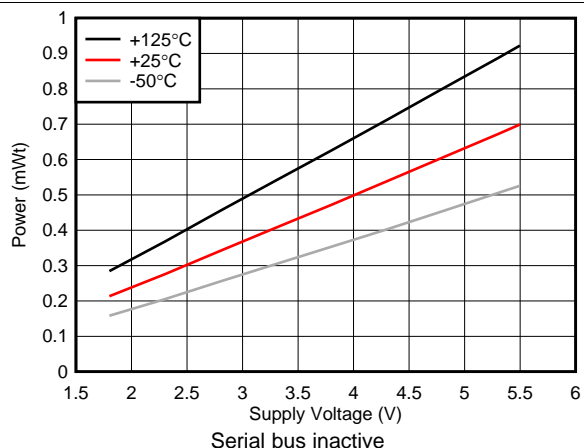


图 12. Power Consumption During Active Conversion

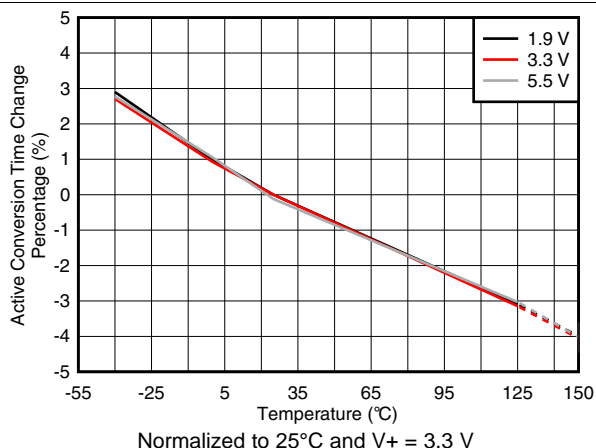


图 13. Active Conversion Time vs Temperature



Typical Characteristics (接下页)

at  $T_A = 25^\circ\text{C}$ ,  $V_+ = 3.3\text{ V}$ , and measurement taken in oil bath (unless otherwise noted)

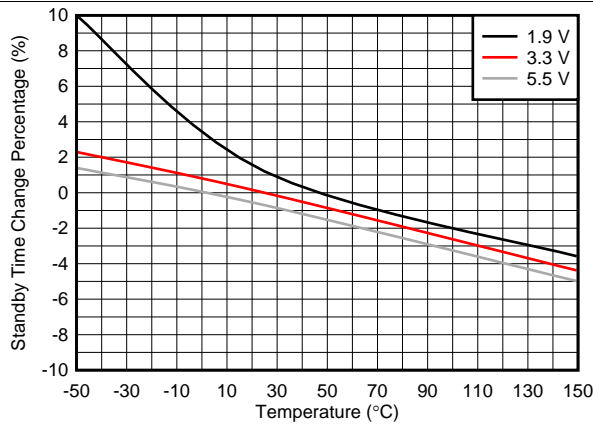


图 14. Standby Time vs Temperature

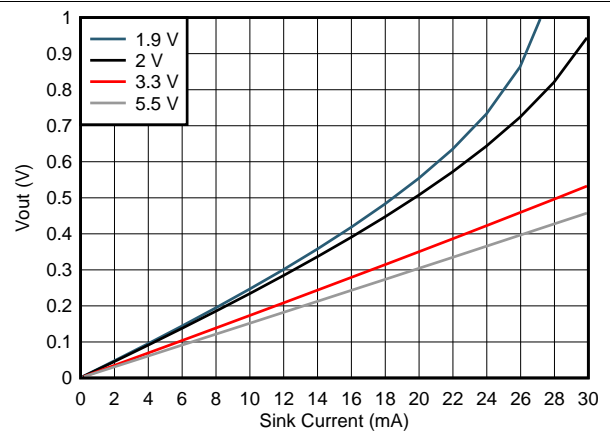


图 15. ALERT Pin Output Voltage vs Pin Sink Current

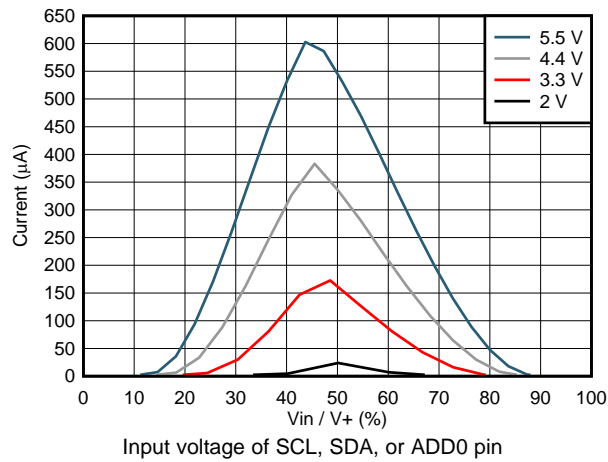


图 16. Supply Current vs Input Cell Voltage

## 7 Detailed Description

### 7.1 Overview

The TMP116 is a digital output temperature sensor that is optimal for thermal-management and thermal-protection applications. The TMP116 is 2-wire, SMBus, and I<sup>2</sup>C interface-compatible. The device is specified over an operating temperature range of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . [图 17](#) shows a block diagram of the TMP116. [图 18](#) shows the ESD protection circuitry contained in the TMP116.

### 7.2 Functional Block Diagrams

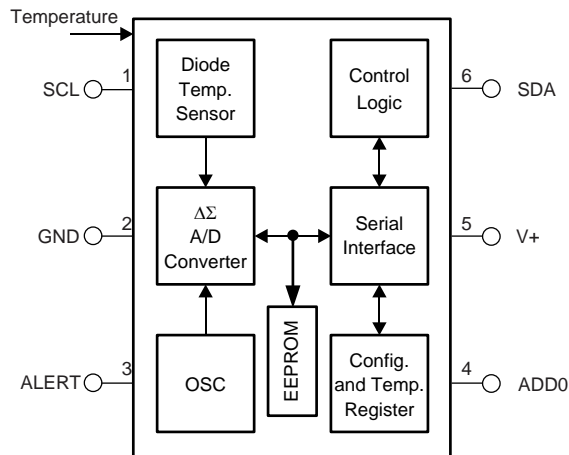


图 17. Internal Block Diagram

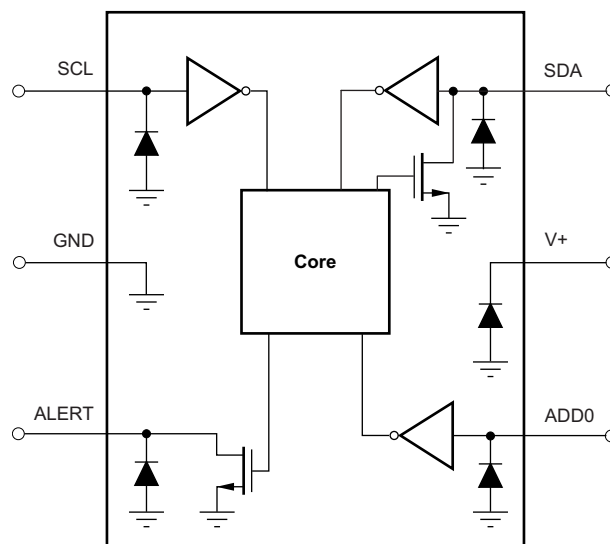


图 18. Equivalent Internal ESD Circuitry

### 7.3 Feature Description

#### 7.3.1 Power Up

After the supply voltage reaches within the operating range, the device requires 1.5 ms to power up before conversions begin. The device can be programmed to startup in shutdown mode as well; see the [EEPROM Programming](#) section. The [temperature register](#) reads  $-256^{\circ}\text{C}$  before the first conversion.

## Feature Description (接下页)

### 7.3.2 Temperature Result and Limits

At the end of every conversion, the device updates the temperature register with the conversion result. The data reading in the result register is in two's complement format, has a data width of 16 bits, and a resolution of 7.8125 m°C. 表 1 shows multiple examples of possible binary data that can be read from the temperature result register and the corresponding hexadecimal and decimal equivalents.

The TMP116 also has alert status flags and alert pin functionality that use the temperature limits stored in the [low limit register](#) and [high limit register](#). The same data format used for the temperature result register can be used for data that are written to the high and low limit registers.

**表 1. 16-Bit Temperature Data Format**

TEMPERATURE (°C)	TEMPERATURE REGISTER VALUE (0.0078125°C RESOLUTION)	
	BINARY	HEX
-256	1000 0000 0000 0000	8000
-25	1111 0011 1000 0000	F380
-0.1250	1111 1111 1111 0000	FFF0
-0.0078125	1111 1111 1111 1111	FFFF
0	0000 0000 0000 0000	0000
0.0078125	0000 0000 0000 0001	0001
0.1250	0000 0000 0001 0000	0010
1	0000 0000 1000 0000	0080
25	0000 1100 1000 0000	0C80
100	0011 0010 0000 0000	3200
255.9921	0111 1111 1111 1111	7FFF

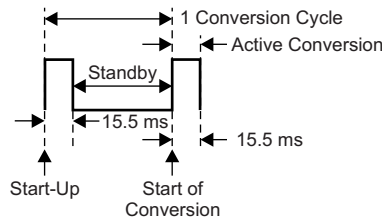
## 7.4 Device Functional Modes

### 7.4.1 Temperature Conversions

The TMP116 can be configured to operate in various conversion modes by using the MOD[1:0] bits. These modes provide flexibility to operate the device in the most power efficient way required for the intended application.

#### 7.4.1.1 Conversion Cycle

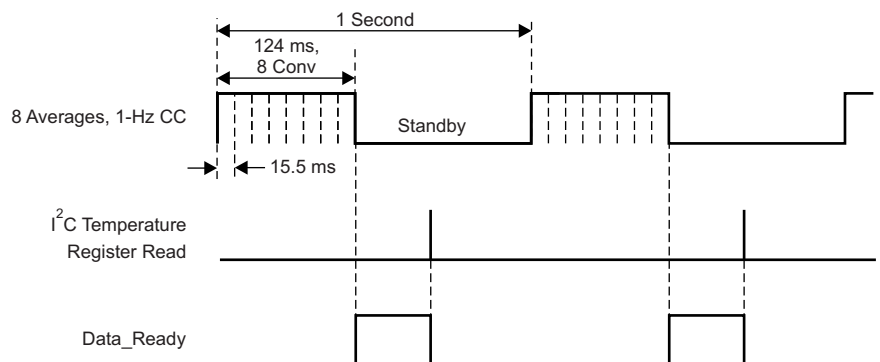
When the device is operating in continuous conversion mode (see the [Continuous Conversion Mode \(CC\)](#) section), every conversion cycle consists of an active conversion period followed by a standby period. During active conversion the device typically consumes 135  $\mu\text{A}$ , and during the low-power standby period the device typically consumes 1.25  $\mu\text{A}$ , as indicated in [表 1](#). [图 19](#) shows a representative current consumption profile of a conversion cycle. The duration of the active conversion period and standby period can be configured using the CONV[2:0] and AVG[1:0] bits in the [configuration register](#), thereby allowing the average current consumption of the device to be optimized based on the application requirements. Changing the conversion cycle period also affects the temperature result update rate because the temperature result register is updated at the end of every conversion.



**图 19. Conversion Cycle Timing Diagram**

#### 7.4.1.2 Averaging

Noise in the conversion result can be improved by configuring the device to report the average of multiple temperature conversions using the AVG[1:0] bits. When the TMP116 is configured to perform averaging, the device executes the configured number of conversions while accumulating the results and reports the average of all conversion results at the end of the process. As illustrated in the noise histograms of [图 6](#) and [图 7](#), the temperature result output has a repeatability of approximately  $\pm 3$  LSBs when there is no averaging and  $\pm 1$  LSB when the device is configured to perform eight averages. As illustrated in [图 20](#), this improvement in noise performance is achieved with the tradeoff of an increase in the active conversion time in a conversion cycle, thereby increasing the average active current consumption. For example, a single active conversion typically takes 15.5 ms so if the device is configured to report an average of eight conversions then the active conversion time is 124 ms (15.5 ms  $\times$  8). Use [公式 1](#) to factor in this increase in active conversion time to accurately calculate the average current consumption of the device. The average current consumption of the device can be decreased by increasing the amount of time the device spends in standby period as compared to active conversion. On reset, the device is configured to report an average of eight conversions with a conversion cycle time of 1 second.



**图 20. Averaging Timing Diagram**

## Device Functional Modes (接下页)

Use [公式 1](#) to calculate the average current consumption of the device in continuous mode.

$$\frac{(\text{Active Current Consumption} \times \text{Active Conversion Time}) + (\text{Standby Current Consumption} \times \text{Standby Time})}{\text{Conversion Cycle Time}}$$

(1)

### 7.4.1.3 Continuous Conversion Mode (CC)

When the MOD[1:0] bits are set to 00, the TMP116 operates in continuous conversion mode. In this mode, the device continuously performs temperature conversions as illustrated in [图 19](#) and updates the temperature result register at the end of every conversion. As described in the [Conversion Cycle](#) section, every conversion cycle consists of an active conversion period followed by a standby period whose duration can be configured using the CONV and AVG bits in the [configuration register](#) based on the temperature accuracy, power consumption, and temperature update rate tradeoffs of the application that the device is used in. At the end of a conversion, the Data\_Ready flag in the configuration register is set. The Data\_Ready flag is cleared by reading the configuration register or the temperature result register. Therefore, the Data\_Ready flag can be used to determine when the conversion completes so that an external controller can synchronize reading the result register with conversion result updates. The state of the Data\_Ready flag can also be monitored on the ALERT pin by setting the DR/nAlert\_EN bit in the configuration register.

### 7.4.1.4 Shutdown Mode (SD)

When 01 is written to the MOD[1:0] bits in the [configuration register](#), the device instantly aborts the currently running conversion and enters a low-power shutdown mode. In this mode, the device powers down all active circuitry and can be used in conjunction with the OS mode to perform temperature conversions. In SD mode, the device typically consumes only 250 nA, which makes the TMP116 suitable for low-power consumption applications, such as battery-operated systems.

### 7.4.1.5 One-Shot Mode (OS)

When in shutdown mode, a single conversion can be performed by writing 10 to MOD[1:0] bits in the [configuration register](#), referred to as a one-shot conversion. After completing a one-shot conversion, the device returns to the low-power shutdown mode. A one-shot conversion cycle only consists of active conversion time and no standby period unlike CC mode. Thus, the duration of a one-shot conversion is only affected by the settings in the AVG bits. The CONV bits do not affect the duration of a one-shot conversion. [图 21](#) shows a timing diagram for this mode with an AVG setting of 00. At the end of a one-shot conversion, the Data\_Ready flag in the configuration register is set. Therefore, the Data\_Ready flag can be used to determine when the conversion completes. The Data\_Ready flag is cleared by performing an I<sup>2</sup>C read on the configuration register or temperature result register. The state of the Data\_Ready flag can also be monitored on the ALERT pin by setting the DR/nAlert\_EN bit in the configuration register.

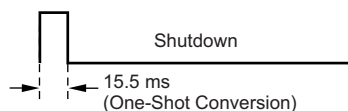


图 21. One-Shot Timing Diagram

## 7.4.2 Therm and Alert Functions

The TMP116 can be used to detect if the temperature has crossed a certain temperature limit or if the device is within a certain temperature range by using the therm or alert functions built into the device. At the end of every conversion, the TMP116 compares the converted temperature result to the values stored in the [low limit register](#) and [high limit register](#) and sets or clears the corresponding status flags in the configuration register, as described in this section.

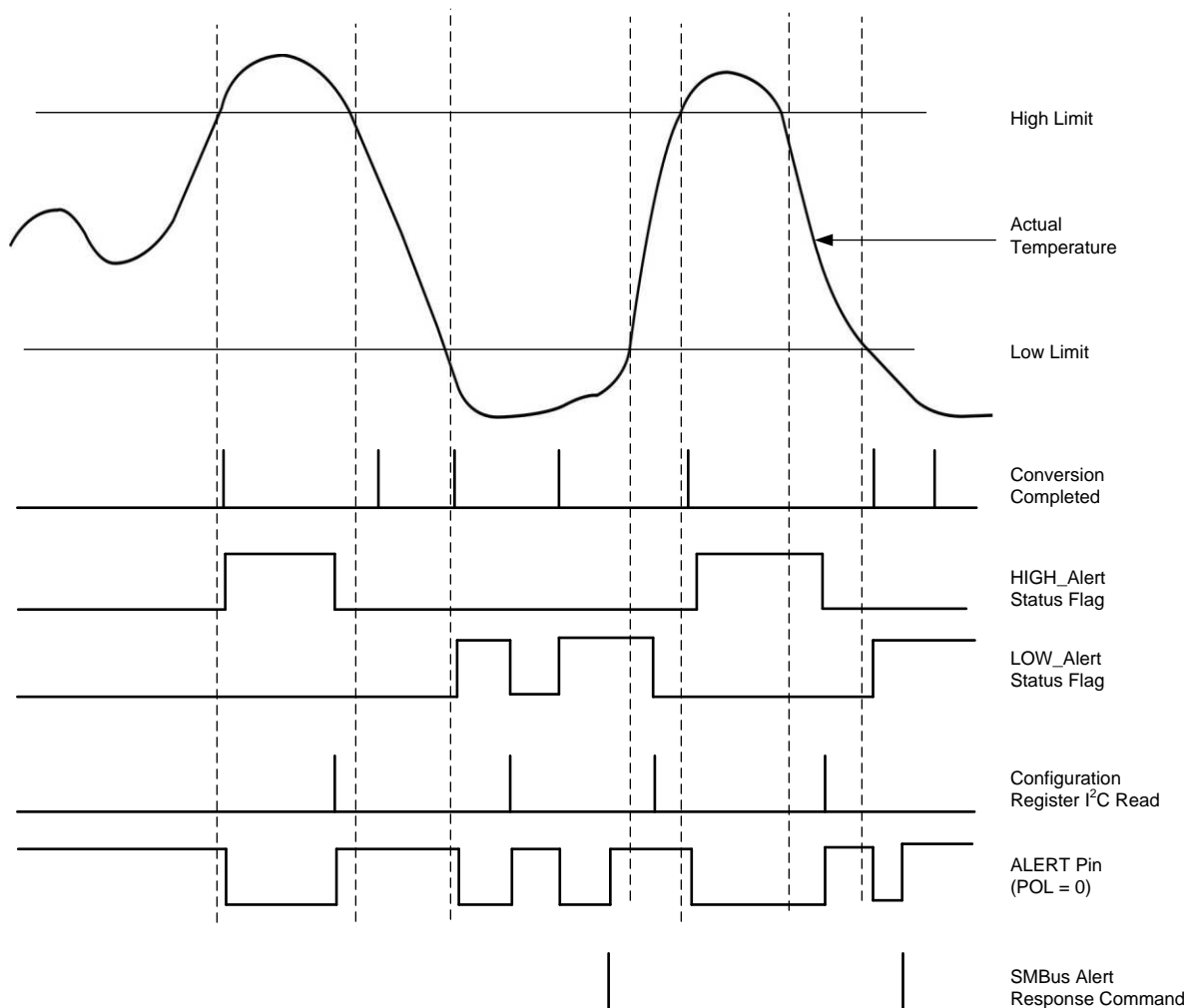
## Device Functional Modes (接下页)

### 7.4.2.1 Alert Mode

When the T/nA bit in the [configuration register](#) is set to 0, the device is in alert mode. In this mode, the device compares the conversion result at the end of every conversion with the values in the [low limit register](#) and [high limit register](#). If the temperature result exceeds the value in the high limit register, the HIGH\_Alert status flag in the configuration register is set. On the other hand, if the temperature result is lower than the value in the low limit register, the LOW\_Alert status flag in the configuration register is set. As shown in [图 22](#), in alert mode the status flags can be cleared by performing an I<sup>2</sup>C read transaction on the configuration register.

Configuring the device in alert mode also affects the behaviour of the ALERT pin. In this mode, the device asserts the ALERT pin when either the HIGH\_Alert or the LOW\_Alert status flag is set as shown in [图 22](#). The ALERT pin can be deasserted by either performing an I<sup>2</sup>C read of the configuration register (which also clears the status flags) or by performing an SMBus alert response command ( see the [SMBus Alert Function](#) section). The polarity of the ALERT pin can be changed by using the POL bit setting in the configuration register.

This mode effectively makes the device behave like a window limit detector and can be used in applications where detecting if the temperature goes outside of the specified range is needed.



**图 22. Alert Mode Timing Diagram**

## Device Functional Modes (接下页)

### 7.4.2.2 Therm Mode

When the T/nA bit in the [configuration register](#) is set to 1 the device is in therm mode. In this mode, the device compares the conversion result at the end of every conversion with the values in the [low limit register](#) and [high limit register](#) and sets the HIGH\_Alert status flag in the configuration register if the temperature exceeds the value in the high limit register. When set, the device clears the HIGH\_Alert status flag if the conversion result goes below the value in the low limit register. Thus, the difference between the high and low limits effectively acts like a hysteresis. In this mode, the LOW\_Alert status flag is disabled and always reads 0. Unlike the alert mode, I<sup>2</sup>C reads of the configuration register do not affect the status bits. The HIGH\_Alert status flag is only set or cleared at the end of conversions based on the value of the temperature result compared to the high and low limits.

As in alert mode, configuring the device in therm mode also affects the behaviour of the ALERT pin. In this mode, the device asserts the ALERT pin if the HIGH\_Alert status flag is set and deasserts the ALERT pin when the HIGH\_Alert status flag is cleared. In therm mode the ALERT pin cannot be cleared by performing an I<sup>2</sup>C read of the configuration register or by performing an SMBus alert response command. As in alert mode, the polarity of the active state of the ALERT pin can be changed by using the POL bit setting in the configuration register.

Thus, this mode effectively makes the device behave like a high-limit threshold detector and can be used in applications where detecting if the temperature has gone above a desired threshold is needed. [图 23](#) shows a timing diagram of this mode.

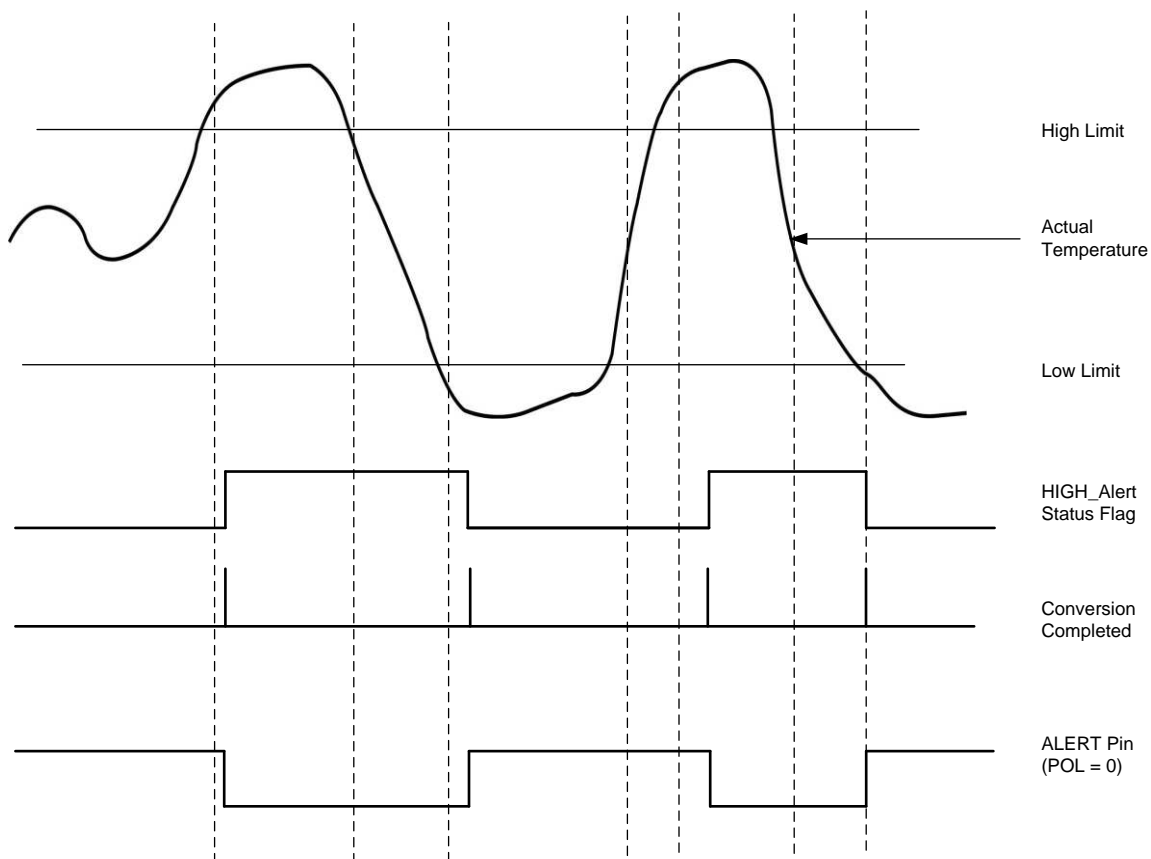


图 23. Therm Mode Timing Diagram

## 7.5 Programming

### 7.5.1 EEPROM Programming

#### 7.5.1.1 EEPROM Overview

The device consists of a user-programmable EEPROM that can be used for two purposes:

- Storing power-on-reset (POR) values of the high limit register, low limit register, conversion cycle time, averaging mode, conversion mode (continuous or shutdown mode), alert function mode (alert or therm mode), and alert polarity
- Four 16-bit locations for general-purpose use; see the [EEPROM\[4:1\] registers](#)

On reset, the device goes through a POR sequence that loads the values programmed in the EEPROM into the respective register map locations. This process takes approximately 1.5 ms. When the power-up sequence is completed the device starts operating in accordance to the configuration parameters that are loaded from the EEPROM. Any I<sup>2</sup>C writes performed during this initial POR period to the limit registers or the configuration register are ignored. I<sup>2</sup>C read transactions can still be performed with the device during the power-up period. While the POR sequence is being executed, the EEPROM\_Busy status flag in the [EEPROM unlock register](#) is set.

During production, the EEPROM in the TMP116 is programmed with reset values as shown in [表 3](#). The [Programming the EEPROM](#) section describes how to change these values. Additionally, during production a unique ID is programmed in the general-purpose EEPROM locations. This unique ID is used to support NIST traceability. The TMP116 units are 100% tested on a production setup that is NIST traceable and verified with equipment that is calibrated to ISO/IEC 17025 accredited standards. Only reprogram the general-purpose EEPROM[4:1] locations if NIST traceability is not desired.

#### 7.5.1.2 Programming the EEPROM

In order to prevent accidental programming, the EEPROM is locked by default. When locked, any I<sup>2</sup>C writes to the register map locations are performed only on the volatile registers and not on the EEPROM.

[图 24](#) illustrates a flow chart describing the EEPROM programming sequence. To program the EEPROM, first unlock the EEPROM by setting the EUN bit in the [EEPROM unlock register](#). After the EEPROM is unlocked, any subsequent I<sup>2</sup>C writes to the register map locations program a corresponding non-volatile memory location in the EEPROM. Programming a single location typically takes 7 ms to complete and consumes 230  $\mu$ A. Do not perform any I<sup>2</sup>C writes until programming is completed. During programming, the EEPROM\_busy flag is set. Read this flag to monitor if the programming is complete. After programming the desired data, issue a general-call reset command to trigger a software reset. The programmed data from the EEPROM are then loaded to the corresponding register map locations as part of the reset sequence. This command also clears the EUN bit and automatically locks the EEPROM to prevent any further accidental programming. Avoid using the device to perform temperature conversions when the EEPROM is unlocked.



Programming (接下页)

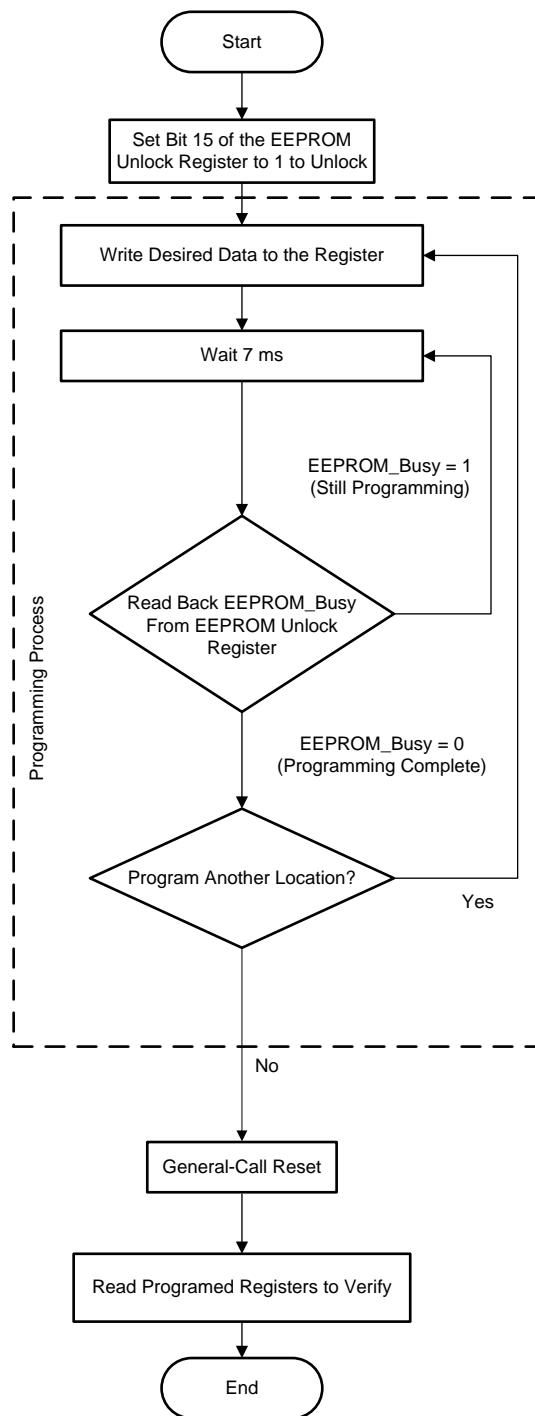


图 24. EEPROM Programming Sequence

## Programming (接下页)

### 7.5.2 Pointer Register

图 25 显示了 TMP116 的内部寄存器结构。该设备的 8 位指针寄存器用于寻址给定的数据寄存器。设备上电复位后的值为 00。默认情况下，TMP116 在上电时读取温度。

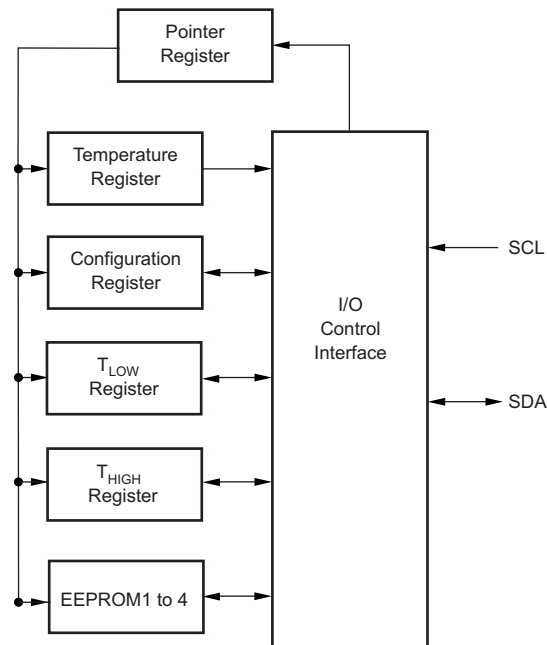


图 25. Internal Register Structures

### 7.5.3 I<sup>2</sup>C and SMBus Interface

#### 7.5.3.1 Serial Interface

The TMP116 operates as a slave device only on the 2-wire, SMBus and I<sup>2</sup>C interface-compatible bus. Connections to the bus are made through the open-drain I/O lines and the SDA and SCL pins. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The device supports the transmission protocol for fast (1 kHz to 400 kHz) mode. Register bytes are sent with the most significant byte first, followed by the least significant byte.

##### 7.5.3.1.1 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data line (SDA) from a high-to low-logic level when the SCL pin is high. All slaves on the bus shift in the slave address byte on the rising edge of the clock, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge and pulling the SDA pin low.

A data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During the data transfer, the SDA pin must remain stable when the SCL pin is high because any change in the SDA pin when the SCL pin is high is interpreted as a START or STOP signal.

When all data are transferred, the master generates a repeated START or STOP condition indicated by pulling the SDA pin from low to high when the SCL pin is high.

## Programming (接下页)

### 7.5.3.1.2 Serial Bus Address

To communicate with the TMP116, the master must first address slave devices through an address byte. The address byte consists of seven address bits and a read-write (R/W) bit indicating the intent of executing a read or write operation.

The TMP116 features an address pin to allow up to four devices to be addressed on a single bus. 表 2 describes the pin logic levels used to properly connect up to four devices. x represents the read-write (R/W) bit.

**表 2. Address Pin and Slave Addresses**

DEVICE TWO-WIRE ADDRESS	ADD0 PIN CONNECTION
1001000x	Ground
1001001x	V+
1001010x	SDA
1001011x	SCL

### 7.5.3.1.3 Writing and Reading Operation

Accessing a particular register on the TMP116 is accomplished by writing the register address to the pointer register. The value for the pointer register is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the TMP116 requires a value for the pointer register.

When reading from the TMP116, the last value stored in the pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. This action is accomplished by issuing an address byte with the R/W bit low, followed by the pointer register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/W bit high to initiate the read command; see 图 28 for details of this sequence. If repeated reads from the same register are desired, continuously sending the pointer register bytes is not necessary because the TMP116 retains the pointer register value until the value is changed by the next write operation.

Register bytes are sent with the most significant byte first, followed by the least significant byte.

### 7.5.3.1.4 Slave Mode Operations

The TMP116 can operate as a slave receiver or slave transmitter. As a slave device, the TMP116 never drives the SCL line.

#### 7.5.3.1.4.1 Slave Receiver Mode

The first byte transmitted by the master is the slave address with the R/W bit low. The TMP116 then acknowledges reception of a valid address. The next byte transmitted by the master is the pointer register. The TMP116 then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The TMP116 acknowledges reception of each data byte. The master can terminate data transfer by generating a START or STOP condition.

#### 7.5.3.1.4.2 Slave Transmitter Mode

The first byte transmitted by the master is the slave address with the R/W bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a *not-acknowledge* on reception of any data byte or by generating a START or STOP condition.

### 7.5.3.1.5 SMBus Alert Function

The TMP116 supports the SMBus alert function. When the ALERT pin is connected to an SMBus alert signal and a master senses that an alert condition is present, the master can send out an SMBus ALERT command (0001 1001) to the bus. If the ALERT pin is active, the device acknowledges the SMBus ALERT command and responds by returning the slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the alert condition is caused by the temperature exceeding  $T_{(HIGH)}$  or falling below  $T_{(LOW)}$ . The LSB is high if the temperature is greater than  $T_{(HIGH)}$ , or low if the temperature is less than  $T_{(LOW)}$ ; see 图 29 for details of this sequence.

If multiple devices on the bus respond to the SMBus ALERT command, arbitration during the slave address portion of the SMBus ALERT command determines which device clears the alert status of that device. The device with the lowest 2-wire address wins the arbitration. If the TMP116 wins the arbitration, the TMP116 ALERT pin becomes inactive at the completion of the SMBus ALERT command. If the TMP116 loses the arbitration, the TMP116 ALERT pin remains active.

### 7.5.3.1.6 General-Call Reset Function

The TMP116 responds to a two-wire, general-call address (0000 000) if the eighth bit is 0. The device acknowledges the general-call address and responds to commands in the second byte. If the second byte is 0000 0110, the TMP116 internal registers are reset to power-up values.

### 7.5.3.1.7 Timeout Function

The TMP116 resets the serial interface if the SCL line is held low by the master or the SDA line is held low by the TMP116 for 35 ms (typical) between a START and STOP condition. The TMP116 releases the SDA line if the SCL pin is pulled low and waits for a START condition from the host controller. To avoid activating the timeout function, maintain a communication speed of at least 1 kHz for the SCL operating frequency.

### 7.5.3.1.8 Timing Diagrams

The TMP116 is 2-wire, SMBus, and I<sup>2</sup>C interface-compatible. 图 26 to 图 30 describe the various operations on the TMP116. Parameters for 图 26 are defined in *Two-Wire Interface Timing*. Bus definitions are:

**Bus Idle:** Both SDA and SCL lines remain high.

**Start Data Transfer:** A change in the state of the SDA line from high to low when the SCL line is high defines a START condition. Each data transfer is initiated with a START condition.

**Stop Data Transfer:** A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

**Data Transfer:** The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The TMP116 can also be used for single byte updates. To update only the MS byte, terminate the communication by issuing a START or STOP communication on the bus.

**Acknowledge:** Each receiving device, when addressed, is obliged to generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a *not-acknowledge* (1) on the last byte transmitted by the slave.

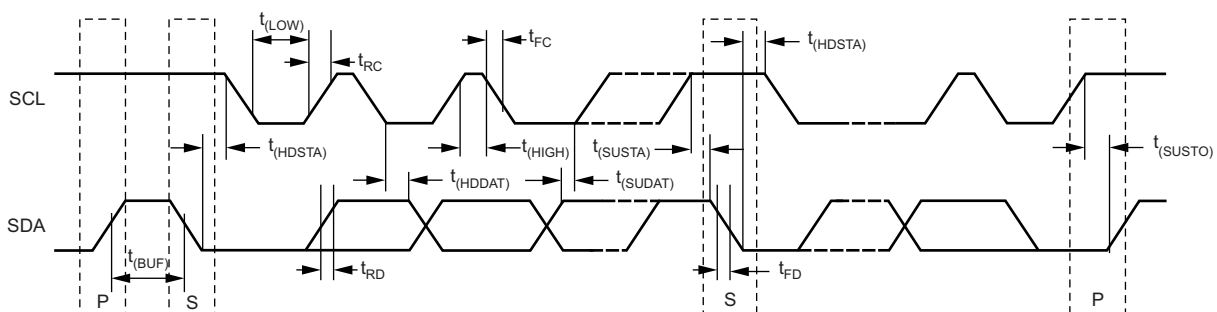


图 26. Two-Wire Timing Diagram

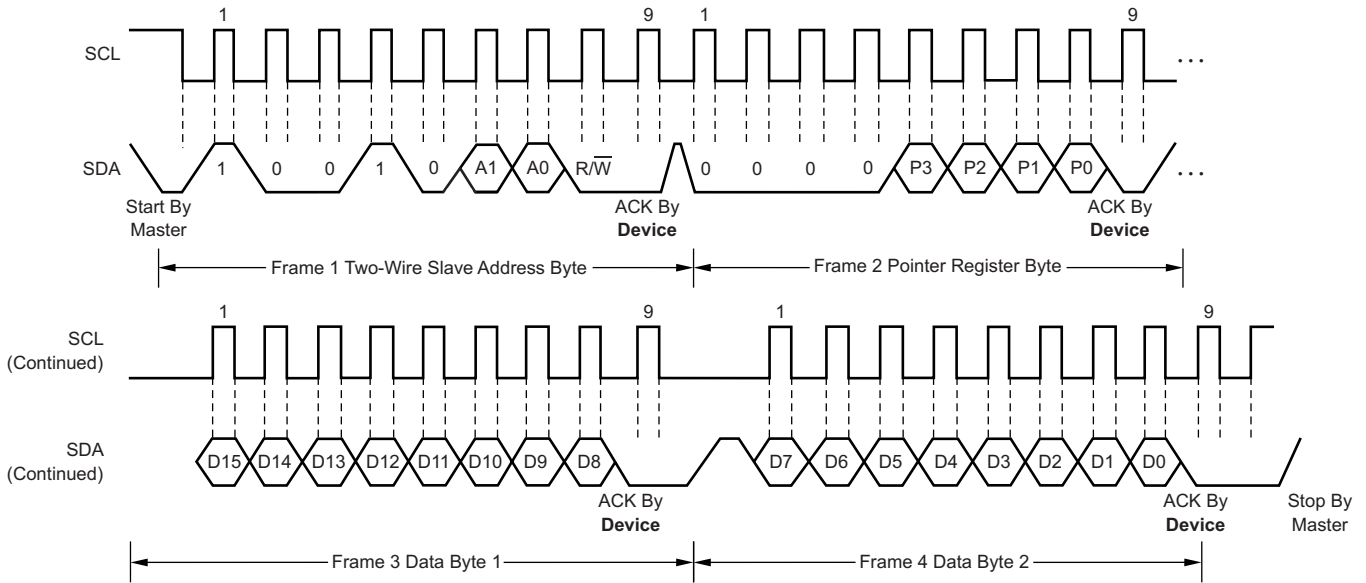


图 27. Write Word Command Timing Diagram

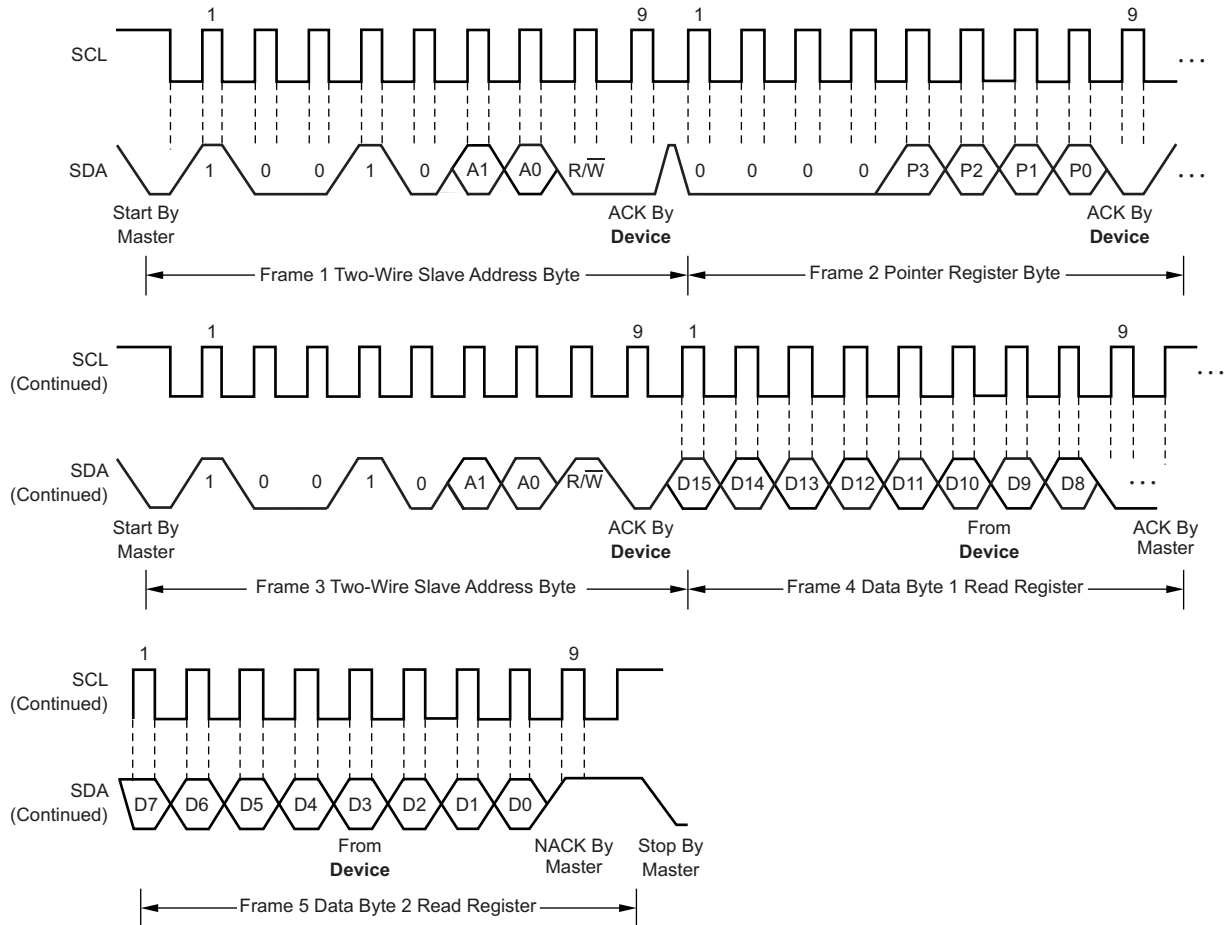


图 28. Read Word Command Timing Diagram

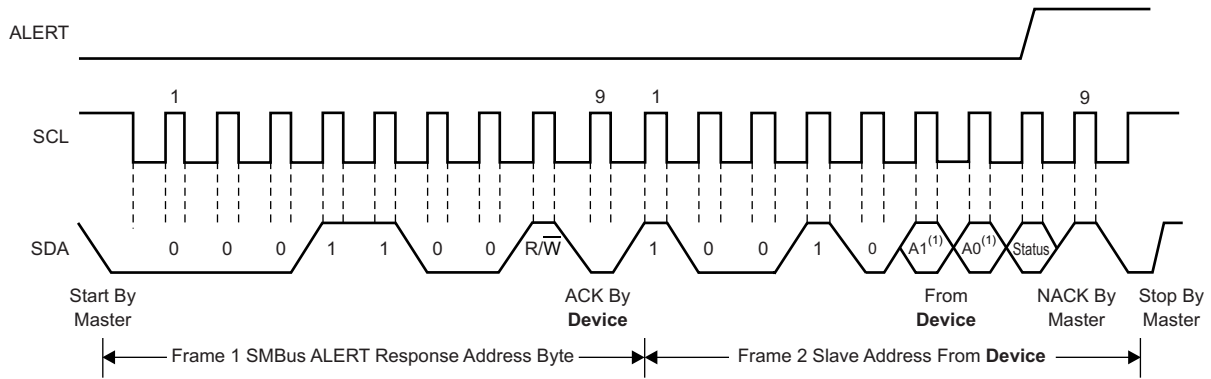


图 29. SMBus ALERT Timing Diagram

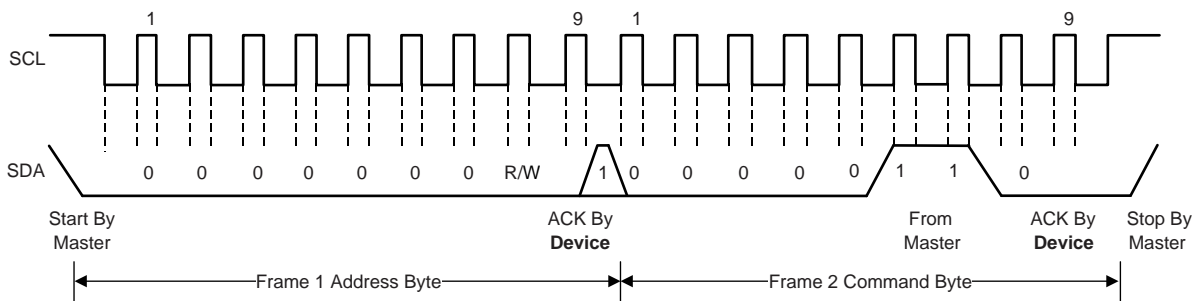


图 30. General-Call Reset Command Timing Diagram

## 7.6 Registers Map

**表 3. Register Map**

ADDRESS (Hex)	DEFAULT VALUE (Hex)	REGISTER DATA																REGISTER NAME
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00h	8000	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	Temperature
01h	0220 <sup>(1)</sup>	HIGH_ Alert	LOW_ Alert	Data_ Ready	EEPROM_ Busy	MOD1	MOD0	CONV2	CONV1	CONV0	AVG1	AVG0	T/nA	POL	DR/nAlert_ EN	—	—	Configuration
02h	6000 <sup>(1)</sup>	H15	H14	H13	H12	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0	High Limit
03h	8000 <sup>(1)</sup>	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0	Low Limit
04h	0000	EUN	EEPROM_ Busy	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EEPROM Unlock
05h	xxxx <sup>(1)</sup>	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	EEPROM1
06h	xxxx <sup>(1)</sup>	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	EEPROM2
07h	0000 <sup>(1)</sup>	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	EEPROM3
08h	xxxx <sup>(1)</sup>	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	EEPROM4
0Fh	x116	—	—	—	—	DID11	DID10	DID9	DID8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0	Device ID

(1) This value is stored in electrically-erasable, programmable read-only memory (EEPROM) during device manufacturing. The device reset value can be changed by writing the relevant code in the EEPROM cells (see the [EEPROM Overview](#) section).

## 7.6.1 Register Descriptions

**表 4. TMP116 Access Type Codes**

Access Type	Code	Description
R	R	Read
Read-write	R/W	Read, write, or both
W	W	Write
-n		Value after reset or the default value

### 7.6.1.1 Temperature Register (address = 00h) [default reset = 8000h]

This register is a 16-bit, read-only register that stores the output of the most recent conversion. One LSB equals 7.8125 m°C. Data are represented in binary two's complement format. Following power-up or a general-call reset, the temperature register reads –256°C until the first conversion is complete (see the [Power Up](#) section).

**图 31. Temperature Register**

15	14	13	12	11	10	9	8
T15	T14	T13	T12	T11	T10	T9	T8
R-1	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
T7	T6	T5	T4	T3	T2	T1	T0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

**表 5. Temperature Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	T[15:0]	R	8000h	16-bit, read-only register that stores the most recent temperature conversion results.



**7.6.1.2 Configuration Register (address = 01h) [default reset = 0220h]**
**图 32. Configuration Register**

15	14	13	12	11	10	9	8
HIGH_Alert	LOW_Alert	Data_Ready	EEPROM_Busy	MOD1 <sup>(1)</sup>	MOD0 <sup>(2)</sup>	CONV2 <sup>(2)</sup>	CONV1 <sup>(2)</sup>
R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0
7	6	5	4	3	2	1	0
CONV0 <sup>(2)</sup>	AVG1 <sup>(2)</sup>	AVG0 <sup>(2)</sup>	T/nA <sup>(2)</sup>	POL <sup>(2)</sup>	DR/Alert <sup>(2)</sup>	—	—
R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R-0	R-0

- (1) The MOD1 bit cannot be stored in EEPROM. The device can only be programmed to start up in shutdown mode or continuous conversion mode.
- (2) These bits can be stored in EEPROM. The factory setting for this register is 0220.

**表 6. Configuration Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	HIGH_Alert	R	0	Alert mode: 1: Set when the conversion result is higher than the high limit 0: Cleared on read of configuration register Therm mode: 1: Set when the conversion result is higher than the therm limit 0: Cleared when the conversion result is lower than the hysteresis
14	LOW_Alert	R	0	Alert mode: 1: Set when the conversion result is lower than the low limit 0: Cleared when the configuration register is read Therm mode: Always set to 0
13	Data_Ready	R	0	Data ready flag. This flag indicates that the conversion is complete and the temperature register can be read. Every time the temperature register or configuration register is read, this bit is cleared. This bit is set at the end of the next conversion when the temperature register is updated. Data ready can be monitored on the ALERT pin by using bit 2 of the configuration register.
12	EEPROM_Busy	R	0	EEPROM busy flag. The value of the flag indicates that the EEPROM is busy during programming or power-up.
11:10	MOD[1:0]	R/W	0	Set conversion mode. 00: Continuous conversion (CC) 01: Shutdown (SD) 10: Continuous conversion (read back = 00) 11: One-shot conversion (OS)
9:7	CONV[2:0]	R/W	100	Conversion cycle bit. See 表 7 for the standby time between conversions.
6:5	AVG[1:0]	R/W	01	Conversion averaging modes. These bits determine the number of conversion results that are collected and averaged before updating the temperature register. The average is an accumulated average and not a running average. 表 8 lists the bit settings for AVG.
4	T/nA	R/W	0	Therm/alert mode select. 1: Therm mode 0: Alert mode
3	POL	R/W	0	ALERT pin polarity bit. 1: Active high 0: Active low
2	DR/Alert	R/W	0	Data ready, ALERT flag select bit. 1: ALERT pin reflects the status of the data ready flag 0: ALERT pin reflects the status of the alert flags
1:0	—	R	0	Not used

**表 7. Conversion Cycle Time in CC Mode**

CONV[2:0]	AVG[1:0] = 00	AVG[1:0] = 01	AVG[1:0] = 10	AVG[1:0] = 11
000	15.5 ms	125 ms	500 ms	1 s
001	125 ms	125 ms	500 ms	1 s
010	250 ms	250 ms	500 ms	1 s
011	500 ms	500 ms	500 ms	1 s
100	1 s	1 s	1 s	1 s
101	4 s	4 s	4 s	4 s
110	8 s	8 s	8 s	8 s
111	16 s	16 s	16 s	16 s

**表 8. AVG Bit Settings**

AVG1	AVG0	DESCRIPTION
0	0	No averaging, 15.5-ms active conversion time
0	1	8 averages, 125-ms active conversion time
1	0	32 averages, 500-ms active conversion time
1	1	64 averages, 1-s active conversion time

### 7.6.1.3 High Limit Register (address = 02h) [reset = 6000h]

This register is a 16-bit, read/write register that stores the high limit for comparison with the temperature result. One LSB equals 7.8125 m°C. The range of the register is  $\pm 256^{\circ}\text{C}$ . Negative numbers are represented in binary two's complement format. Following power-up or a general-call reset, the high-limit register is loaded with the stored value from the EEPROM that is set as factory default to 6000h.

**图 33. High Limit Register**

15	14	13	12	11	10	9	8
H15	H14	H13	H12	H11	H10	H9	H8
R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
H7	H6	H5	H4	H3	H2	H1	H0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**表 9. High Limit Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	H[15:0]	R/W	6000h	16-bit, read/write register that stores the high limit for comparison with the temperature result.

### 7.6.1.4 Low Limit Register (address = 03h) [reset = 8000h]

This register is configured as a 16-bit, read/write register that stores the low limit for comparison with the temperature result. One LSB equals 7.8125 m°C. The range of the register is  $\pm 256^{\circ}\text{C}$ . Negative numbers are represented in binary two's complement format. Following power-up or reset, the low-limit register is loaded with the stored value from the EEPROM that is set in the factory to 8000h.

**图 34. Low Limit Register**

15	14	13	12	11	10	9	8
L15	L14	L13	L12	L11	L10	L9	L8
R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
L7	L6	L5	L4	L3	L2	L1	L0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**表 10. Low Limit Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	L[15:0]	R/W	8000h	16-bit, read/write register that stores the low limit for comparison with the temperature result.

**7.6.1.5 EEPROM Unlock Register (address = 04h) [reset = 0000h]**

**图 35. EEPROM Unlock Register**

15	14	13	12	11	10	9	8
EUN	EEPROM_Busy	—	—	—	—	—	—
R/W-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

**表 11. EEPROM Unlock Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	EUN	R/W	0	EEPROM unlock. 0: EEPROM is locked for programming: writes to all EEPROM addresses (such as configuration, limits, and EEPROM locations 1-4) are written to registers in digital logic and are not programmed in the EEPROM 1: EEPROM unlocked for programming: any writes to writable registers program the respective location in the EEPROM
14	EEPROM_Busy	R	0	EEPROM busy. This flag is the mirror of the EEPROM busy flag (bit 12) in the configuration register. 0: Indicates that the EEPROM is ready, which means that the EEPROM has finished the last transaction and is ready to accept new commands 1: Indicates that the EEPROM is busy, which means that the EEPROM is currently completing a program or power-up on reset load
13:0	—	R	0	Not used

**7.6.1.6 EEPROM1 Register (address = 05h) [reset = 0000h]**

The EEPROM1 register is a 16-bit register that be used as a scratch pad by the customer to store general-purpose data. This register has a corresponding EEPROM location. Writes to this address when the EEPROM is locked write data into the register and not to the EEPROM. Writes to this register when the EEPROM is unlocked causes the corresponding EEPROM location to be programmed; see the [Programming the EEPROM](#) section. EEPROM[4:1] are preprogrammed during manufacturing with the unique ID that can be overwritten. In order to support NIST traceability, do not delete or reprogram EEPROM[4:1].

**图 36. EEPROM1 Register**

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x

**表 12. EEPROM1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	D[15:0]	R/W	xxxxh	This 16-bit register is to be used as a scratch pad by the customer.

**7.6.1.7 EEPROM2 Register (address = 06h) [reset = 0000h]**

This register function the same as the EEPROM1 register.

**图 37. EEPROM2 Register**

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x

**表 13. EEPROM2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	D[15:0]	R/W	xxxxh	This 16-bit register is to be used as a scratch pad by the customer.

**7.6.1.8 EEPROM3 Register (address = 07h) [reset = 0000h]**

This register function is the same as the EEPROM1 register.

**图 38. EEPROM3 Register**

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

**表 14. EEPROM3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	D[15:0]	R/W	0	This 16-bit register is to be used as a scratch pad by the customer.

**7.6.1.9 EEPROM4 Register (address = 08h) [reset = xxxh]**

This register function is the same as the EEPROM1 register.

**图 39. EEPROM4 Register**

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x

**表 15. EEPROM4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	D[15:0]	R/W	xxxh	This 16-bit register is to be used as a scratch pad by the customer.

**7.6.1.10 Device ID Register (address = 0Fh) [reset = x116h]**

This read-only register indicates the device ID.

**图 40. Device ID Register**

15	14	13	12	11	10	9	8
—	—	—	—	DID11	DID10	DID9	DID8
R-x	R-x	R-x	R-x	R-0	R-0	R-0	R-1
7	6	5	4	3	2	1	0
DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
R-0	R-0	R-0	R-1	R-0	R-1	R-1	R-0

**表 16. Device ID Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:12	—	R	x	Not used.
11:0	DID[11:0]	R	116h	These bits indicate the device ID.

## 8 Application and Implementation

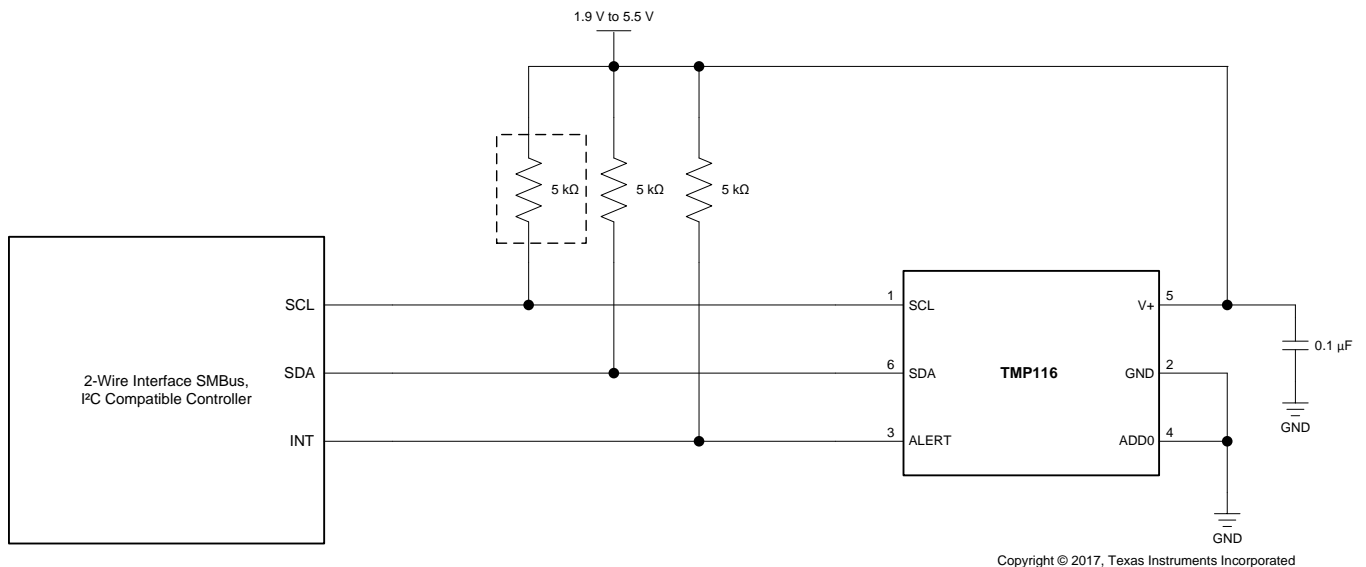
### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TMP116 is used to measure the temperature of the board location where the device is mounted. The programmable address options allow up to four locations on the board to be monitored on a single serial bus.

#### 8.1.1 Typical Application



NOTE: The SDA and ALERT pins require pullup resistors.

图 41. Typical Connections

##### 8.1.1.1 Design Requirements

The TMP116 operates only as a slave device and communicates with the host via the I<sup>2</sup>C-compatible serial interface. SCL is the input pin, SDA is a bidirectional pin, and ALERT is the output. The TMP116 requires a pullup resistor on the SCL, SDA, and ALERT pins. The recommended value for the pullup resistors is 5 kΩ. In some applications the pullup resistor can be lower or higher than 5 kΩ. A 0.1-μF bypass capacitor is recommended to be connected between V+ and GND. An SCL pullup resistor is required if the system microprocessor SCL pin is open-drain. Use a ceramic capacitor type with a temperature rating from -40°C to +125°C, placed as close as possible to the V+ pin of the TMP116. The decoupling capacitor reduces any noise induced by the system. When connected directly to GND, V+, SDA, and SCL, use the ADD0 pin for address selection for configuring four possible unique slave ID addresses; 表 1 explains the addressing scheme. The ALERT output pin can be connected to a microcontroller interrupt that triggers an event that occurred when the temperature limit exceeds the programmable value in registers 02h and 03h. The ALERT pin can be left floating if not in use or connected to ground.

## Application Information (接下页)

### 8.1.1.2 Detailed Design Procedure

#### 8.1.1.2.1 TMP116 Design Procedure

The TMP116 is a local temperature sensor. Measuring a temperature point with a surface-mount device is very challenging because of the external influence of surrounding air and other components. The TMP116 mainly monitors the PCB temperature at the desired hotspot. To maintain accuracy in applications that requires surface temperature measurement, follow good layout techniques (such as understanding the dominant thermal path, isolating the island surround by the package, and keeping the distance as far as possible from the heat source).

For sensors in plastic packages (such as the TMP116 DFN device), 图 42 shows that the die attach pad (DAP) provides the most dominant thermal path. With the DAP, a board-mounted sensor usually does an excellent job of measuring board temperature. The die sits on top of the metal plate leadframe with a non-conductive die adhesive in between, allowing for a fast thermal response.

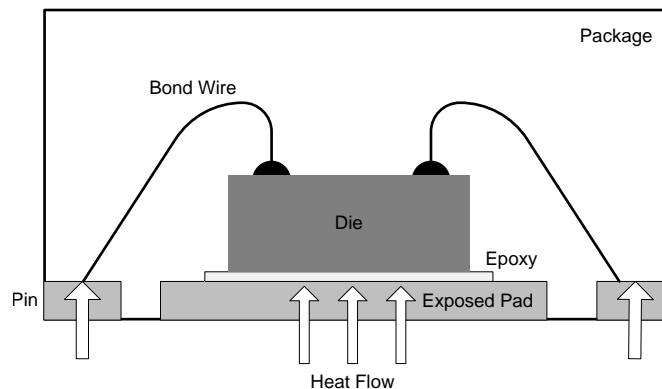


图 42. WSON Package Cross Section

Most power-hungry electronic components such as processor chips, field programmable gate arrays (FPGAs), application-specific integrated circuits (ASICs), and voltage regulators heat up during operation. In order to accurately measure the ambient temperature of a sensor in a plastic package, isolate the sensor from the heat source using isolation island techniques and distance. TI recommends two vias per TMP116 dimension of the thermal pad. The DAP and two vias help improve thermal characteristics. Thus, in order to take advantage of this feature, mount the TMP116 on the board with the two copper planes on the top and bottom of the via of equal length as the exposed die attach dimension. The bottom plane contains the temperature sensing elements. In order to achieve the fast temperature response, the mini board dimension must be enough to accommodate the TMP116 and the bypass capacitor with the isolation air gap to prevent the heat source dissipated to the mini sub-board.

#### 8.1.1.2.2 Noise and Averaging

The device temperature sampling distribution (without internal averaging) covers an area of approximately six neighboring codes. The noise area of the six codes remains the same at full supply and full temperature range with a standard deviation of approximately 1 LSB. The device provides an averaging tool for 8, 32, and 64 samples. As illustrated in 图 7, even the 8-sample averaging reduces the internal noise distribution to a theoretical minimum of 2 LSB. This averaging means that if the system temperature slowly changes and the supply voltage is stable, then the 8-sample averaging can be enough to neutralize the device noise and provide stable temperature readings. However, if the system temperature is noisy (such as when measuring air flow temperatures), than higher averaging numbers are recommended to be used.



## Application Information (接下页)

### 8.1.1.2.3 Self-Heating Effect (SHE)

During ADC conversion some power is dissipated that heats the device despite the small power consumption of the TMP116. Consider the self-heating effect (SHE) for certain precise measurements. 图 43 shows the device SHE in still air at 25°C after the supply is switched on. The device package, including the thermo pad, is soldered to the 11-mm x 20-mm x 1.1-mm size coupon board. The board is located horizontally, with the device on top. The TMP116 is in continuous conversion mode with 64 sampling averaging and zero conversion cycle time. There is no digital bus activity aside from reading temperature data one time each second. As shown in 图 43, the SHE stabilization time in still air is greater when the device dissipates more power.

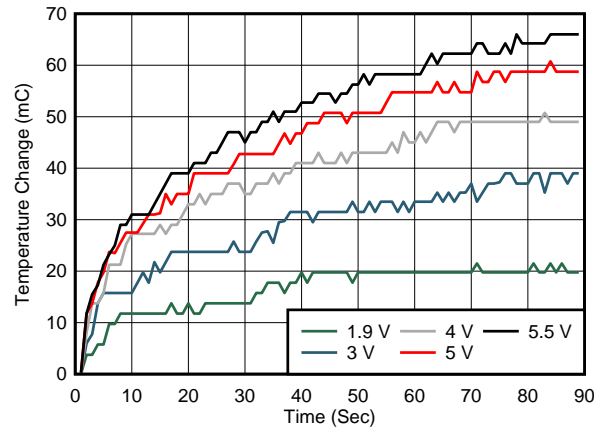


图 43. Self-Heating in Still Air versus Temperature and Dissipated Power

The SHE drift is strongly proportional to the device dissipated power. The SHE drift is also proportional to the device temperature because the consumption current with the same supply voltage increases with temperature. 图 44 shows the SHE drifts versus temperature and dissipated power at 25°C for the same coupon board and the same conditions described previously.

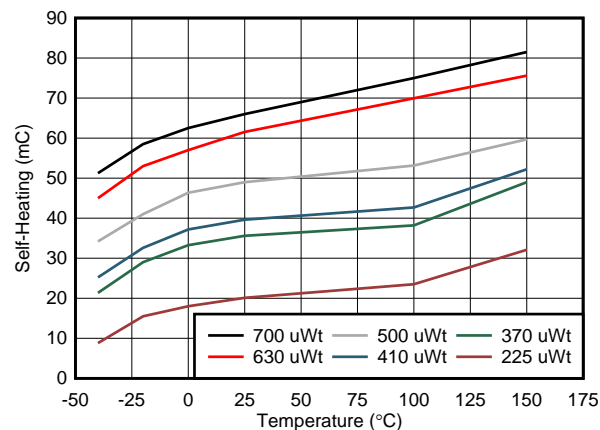


图 44. Self-Heating in Still Air vs Temperature and Dissipated Power at 25°C

To estimate the SHE for similar size boards, calculate the device consumption power for 25°C and use the corresponding power line shown in 图 44. For example, in CC mode without dc at a 3.3-V supply at 25°C, the device dissipates 410  $\mu$ Wt. So self-heating in still air is approximately 40 m°C for the described condition.

## Application Information (接下页)

The following methods can reduce the SHE:

- System calibration removes not only the self-heating error and power-supply rejection ratio (PSRR) effect but also compensates the temperature shift caused by the thermal resistance between the device and the measured object.
- If practical, use the device one-shot mode. If continuous conversion is needed, use the conversion cycle mode with significant standby time. For example, in most cases an 8-sample averaging (125 ms) with a 1-second conversion cycle provides enough time for the device to cool down to the environment temperature and removes the SHE.
- Use the minimal acceptable power supply voltage.
- Use a printed-circuit board (PCB) layout that provides minimal thermal resistance to the device.
- Avoid using small-value pullup resistors on the SDA and ALERT pins. Instead, use pullup resistors larger than 2 k $\Omega$ .
- Ensure that the SCL and SDA signal levels remain below 10% or above 90% of the device supply voltage.
- Avoid heavy bypass traffic on the data line. Communication to other devices on the same data line increases the supply current even if the device is in SD mode.
- Use the highest available communication speed.

### 8.1.1.2.4 Synchronized Temperature Measurements

When four temperature measurements are needed in four different places simultaneously, triggering a reset is recommended. In this method, four devices are programmed with control registers set to CC mode with a conversion cycle time of 16 s. All four devices are connected to same 2-wire bus with four different bus addresses. The bus general-call reset command is issued by the master. This command triggers all devices to reset (which takes approximately 1.5 ms) and triggers a simultaneous temperature sampling according to configuration registers setting. The master has 16 seconds to read data from the devices.

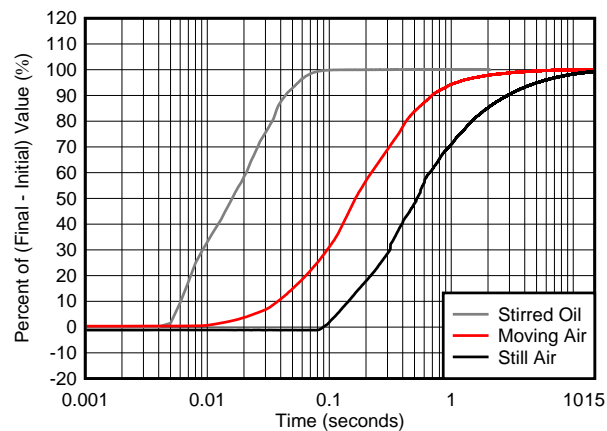
## Application Information (接下页)

### 8.1.1.3 Application Curve

图 45 显示了 TMP116 对温度变化的反应速度。进行热响应实验时必须考虑两个因素：热导率和热质量。热导率是衡量材料（如静止空气或搅拌油）传导热量能力的度量。热导率主要用于描述热量如何通过材料传导。较高的值反映了更高的传热效率。一个好的布局技术是保持热质量尽可能小。较小的热质量会导致更好的热响应。

这些实验的目的是调查需要多长时间才能使 TMP116 温度达到设定温度并稳定。有三种类型的测试用于热响应：静止空气、流动空气和搅拌油，如图 45 所示。该图显示了 TMP116 封装在静止空气室中、在风洞中流动空气以及在油浴中（分别对应各自的曲线）在 70°C 温度环境中从室温（23°C）的阶跃响应。达到输入阶跃 63% 的时间常数取决于测试类型。时间常数结果取决于 PCB 和 TMP116 所安装板的厚度。对于此测试，使用 TMP116EVM 进行热响应测试。TMP116EVM 的尺寸为 7.6 mm × 17.8 mm，厚度为 1 mm。

在所有方法中，静止空气的热响应最慢，因为它是将盒子放在烤箱内部而没有任何辅助元素，而搅拌油实验则给出了最快的热响应时间。



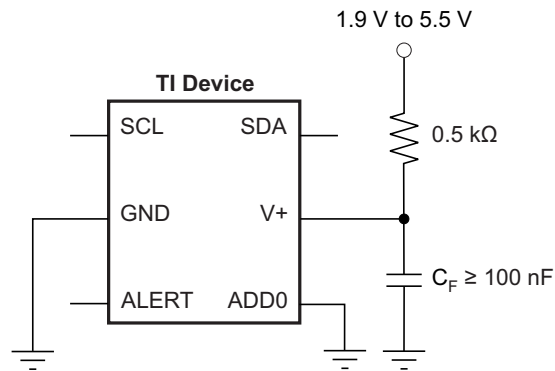
$$V+ = 3.3 \text{ V}, t_{\text{INITIAL}} = 23^{\circ}\text{C}, t_{\text{FINAL}} = 70^{\circ}\text{C}$$

图 45. Thermal Response

## 9 Power Supply Recommendations

The TMP116 operates on a power-supply range from 1.9 V to 5.5 V. The device is trimmed for operation at a 3.3-V supply, but can measure temperature accurately in the full supply range. A power-supply bypass capacitor is required, which must be placed as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 100 nF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

The TMP116 is a very low-power device and generates low noise on the supply bus. Applying an RC filter to the V+ pin of the device can further reduce any noise that the TMP116 might propagate to other components.  $R_F$  in [Figure 46](#) must be less than 0.5 k $\Omega$  and  $C_F$  must be at least 100 nF. The package thermal pad is not connected to the device ground and can be left floating for convenience or grounded for better thermal resistance.



**图 46. Noise-Reduction Techniques**

## 10 Layout

### 10.1 Layout Guidelines to Achieve a High-Precision Temperature Reading

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1  $\mu$ F. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. In some cases the pullup resistor can be the heat source, therefore, maintain some distance between the resistor and the device.

Mount the TMP116 on the PCB pad to provide the minimum thermal resistance to the measured object surface or to the surrounding air. The recommended PCB layout minimizes the device self-heating effect, reduces the time delay as temperature changes, and minimizes the temperature offset between the device and the object.

1. The device thermal pad has a direct thermal contact to the die; therefore, soldering is essential to minimize thermal resistance from the sensor to the PCB. The recommendations are:
  - Solder the package thermal pad to the corresponding PCB pad.
  - Extend the PCB pad outside the package, if possible.
  - Place thermal pads on the top and bottom of the PCB and connect pads through vias. (Vias typically have four times less thermal resistance than the same area of the PCB board.)
  - Fill vias with metal, if possible.
  - The thermal pad can be left floating.
2. Minimize thermal resistance from the PCB to the environment:
  - Design the pin-soldering pads to be as large as possible, especially if these pads are corner pads.
  - Use a PCB with thicker copper layers, when possible.
  - If the PCB has unused internal layers, extend these layers under the TMP116.
  - Cover the top and bottom unused board space with the copper layer.

## Layout Guidelines to Achieve a High-Precision Temperature Reading (接下页)

3. If the device is used to measure air temperature:
  - Miniaturize the board to reduce thermal mass. Smaller thermal mass results in better thermal response.
  - Place two copper planes of equal size to the top and bottom of the exposed pad.
  - Remove the top solder mask.
  - To prevent oxidation, cover any exposed copper with solder paste.
  - Thermal isolation is required to avoid thermal coupling from heat source components through the PCB.
  - Avoid running the copper plane underneath the temperature sensor.
  - Maximize the air gap between the sensor and the surrounding copper areas (anti-etch), especially when close to the heat source.
  - Create a PCB cutout between sensor and other circuits. Leave a narrow channel away from heat source components as a routing bridge into the island.
  - If the heat source is top side, avoid running traces on top; instead, route all signals on the bottom side.
  - Place the board vertically to improve air flow and to reduce dust collection.

### 10.2 Layout Example

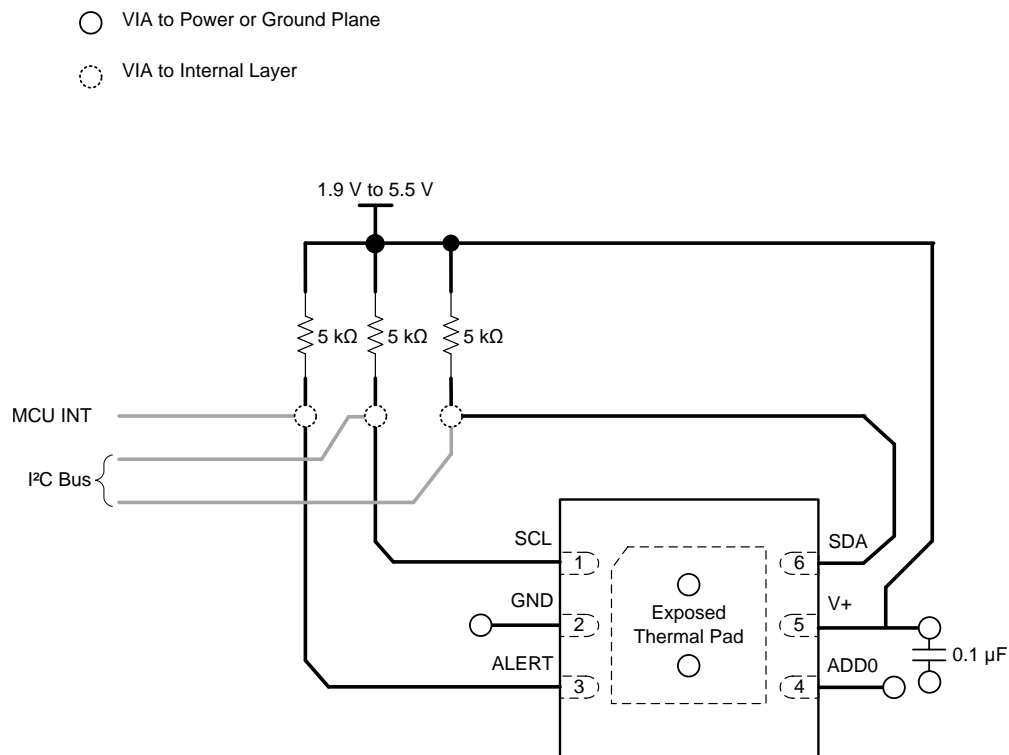


图 47. Layout Recommendation

## 11 器件和文档支持

### 11.1 文档支持

#### 11.1.1 相关文档

相关文档请参阅以下部分：

- 配备采用行业标准 **LM75** 外形尺寸和引脚排列的 **I<sup>2</sup>C** 和 **SMBus** 接口的 **TMPx75** 温度传感器
- 配备采用行业标准 **LM75** 外形尺寸和引脚排列的 **I2C** 和 **SMBus** 接口的 **TMP275 ±0.5°C** 温度传感器

### 11.2 接收文档更新通知

如需接收文档更新通知，请访问 [www.ti.com.cn](http://www.ti.com.cn) 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

### 11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 商标

E2E is a trademark of Texas Instruments.

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### 11.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP116AIDRVR	ACTIVE	WSO	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 150	T116	<a href="#">Samples</a>
TMP116AIDRVT	ACTIVE	WSO	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 150	T116	<a href="#">Samples</a>
TMP116NAIDRVR	ACTIVE	WSO	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 150	116N	<a href="#">Samples</a>
TMP116NAIDRVT	ACTIVE	WSO	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 150	116N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## GENERIC PACKAGE VIEW

DRV 6

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4206925/F



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NOTES:

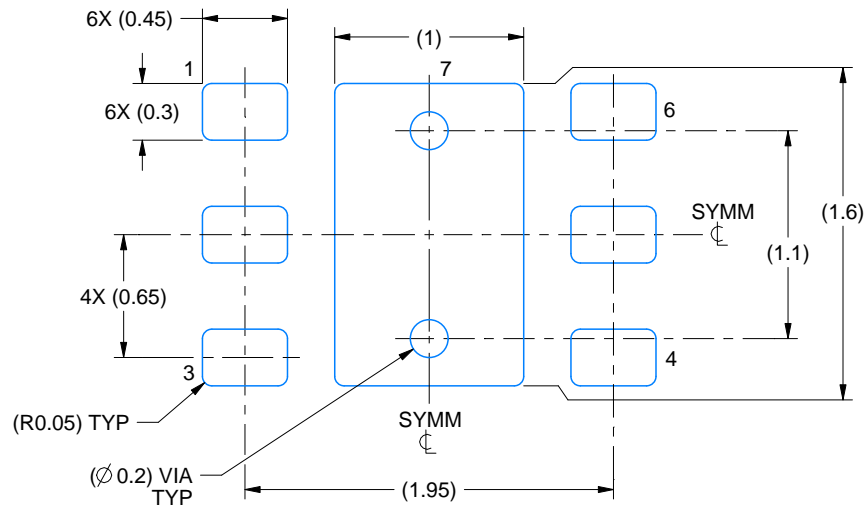
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

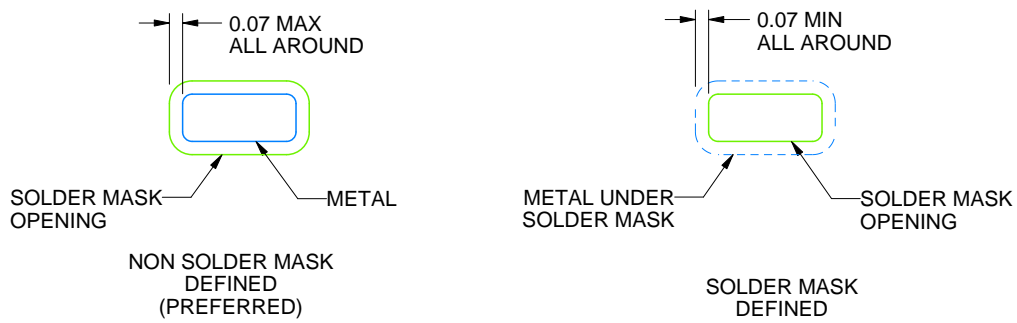
DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7  
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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