GL14P04-8

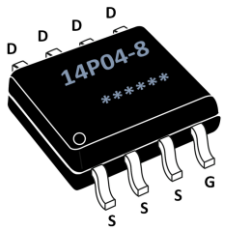
GL Silicon P-Channel Power MOSFET

General Description:

The GL14P04-8 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is SOP-8, which accords with the RoHS standard.

V_{DSS}	-40	V
I_D	-14	A
P_D	3.0	W
$R_{DS(ON)type}$	9	mΩ

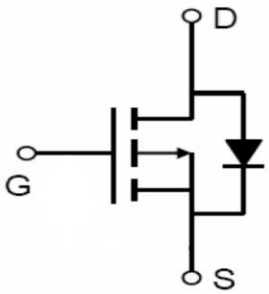
SOP-8



Features:

- $R_{DS(ON)}$ <11mΩ @ V_{GS}=10V (Typ9mΩ)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Inner Equivalent Principium Chart



Applications:

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Absolute (Tc= 25℃ unless otherwise specified):

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	-40	V
I_D	Continuous Drain Current	-14	A
	Continuous Drain Current T_C = 70 °C	-12	A
I_{DM} [a1]	Pulsed Drain Current	-56	A
V_{GS}	Gate-to-Source Voltage	±20	V
Eas [a5]	L=0.5mH	180	mJ
dv/dt [a3]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	3.0	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, –55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃

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Electrical Characteristics (Tc= 25℃ unless otherwise specified):

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	-40	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=-40V, V_{GS}= 0V,T_a=25℃	--	--	1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+20V	--	--	0.1	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-20V	--	--	-0.1	μA

ON Characteristics[a3]						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=-10V,I_D=-14A	--	9	11	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	-1	--	-3.0	V
Pulse width tp≤380μs,δ≤2%						

Dynamic Characteristics[a4]						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	V_{DS}=-5V,I_D=-14A	25	--	--	S
C_{iss}	Input Capacitance	V_{GS}=0V,V_{DS}=-15V f=1.0MHz	--	5100	--	pF
C_{oss}	Output Capacitance		--	570	--	
C_{rss}	Reverse Transfer Capacitance		--	480	--	

Resistive Switching Characteristics[a4]						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=-15V,I_D=-14A V_{GS}=-10V,R_G=3Ω	--	15	--	ns
t_r	Rise Time		--	12	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	70	--	
t_f	Fall Time		--	18	--	
Q_g	Total Gate Charge	V_{DD}=-15V, I_D=-14A V_{GS}=-10V	--	102	--	nC
Q_{gs}	Gate to Source Charge		--	22	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	27	--	

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Source-Drain Diode Characteristics

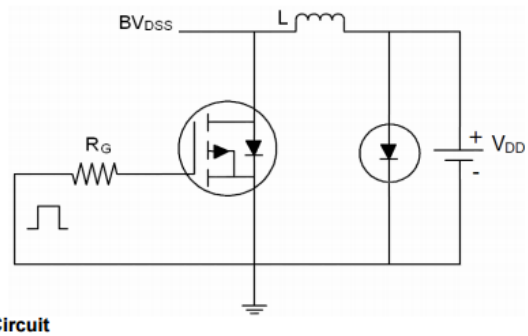
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current [a2](Body Diode)		--	--	-14	A
V_{SD}	Diode Forward Voltage[a3]	I_S=-14A,V_{GS}=0V	--	--	-1.5	V
t_{rr}	Reverse Recovery Time	I_S=-14A,T_j = 25° C	--	38	--	ns
Q_{rr}	Reverse Recovery Charge	dI_F/dt=100A/us,V_{GS}=0V	--	30	--	nC

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case[a2]	41.7	℃/W

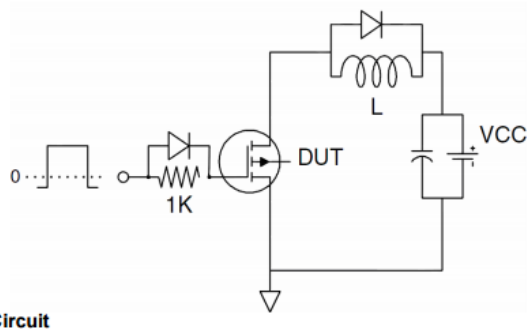
[a1]: Repetitive Rating: Pulse width limited by maximum junction temperature.
[a2]: Surface Mounted on FR4 Board, t≤10sec.
[a3]: Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%.
[a4]: Guaranteed by design, not subject to production
[a5]: T_J=25℃, V_{DD}=15V, V_G=10V,L=0.5Mh

Test Circuit

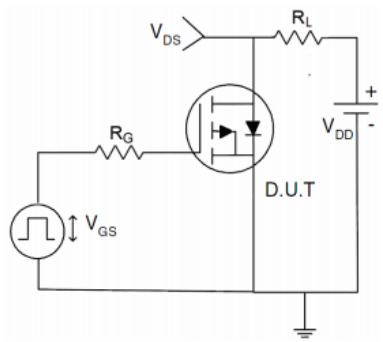
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

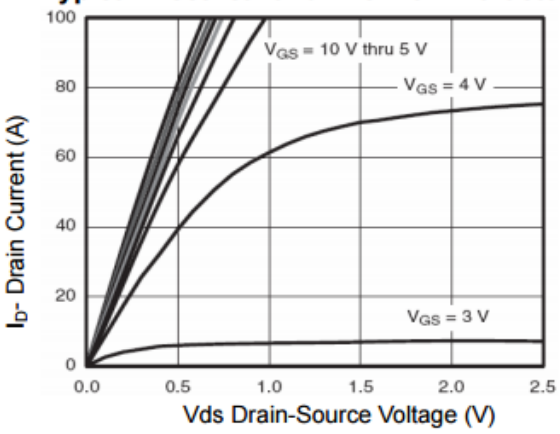


Figure 1 Output Characteristics

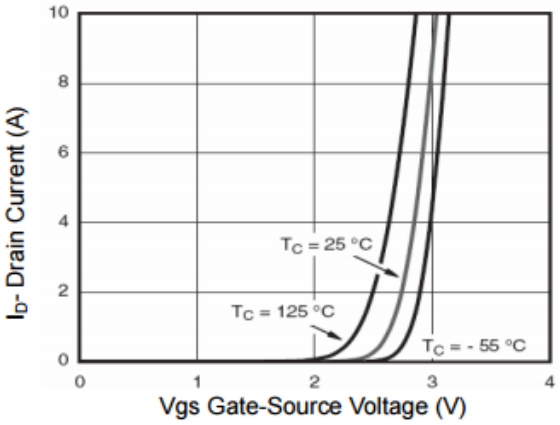


Figure 2 Transfer Characteristics

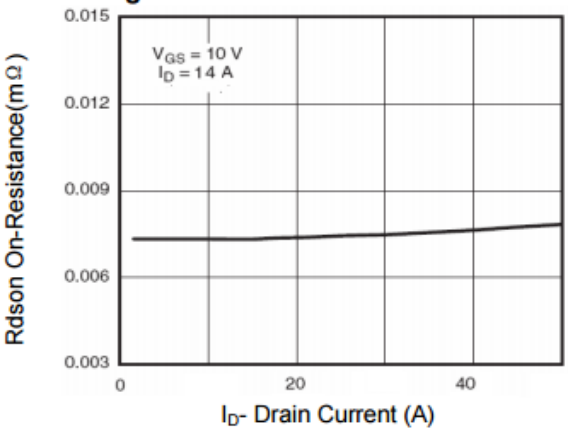


Figure 3 Rdson- Drain Current

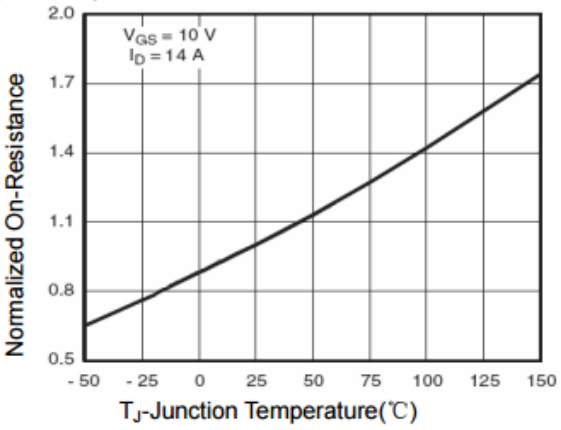


Figure 4 Rdson-Junction Temperature

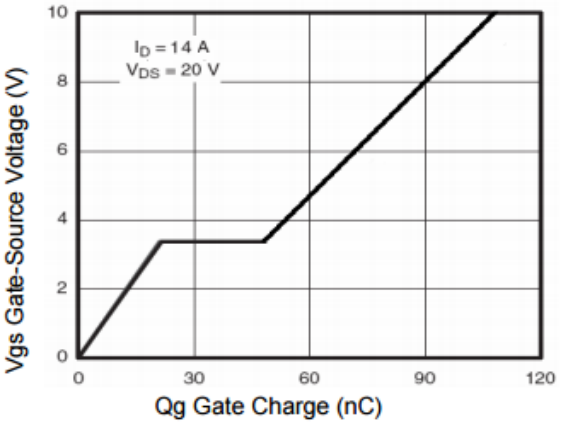


Figure 5 Gate Charge

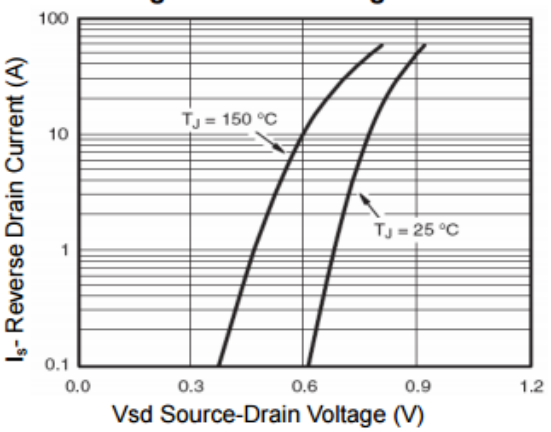


Figure 6 Source- Drain Diode Forward

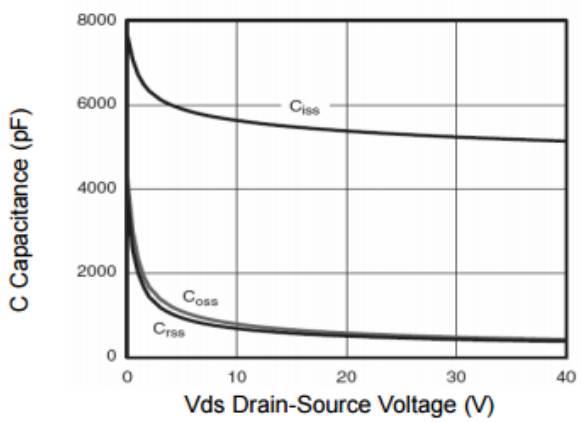


Figure 7 Capacitance vs Vds

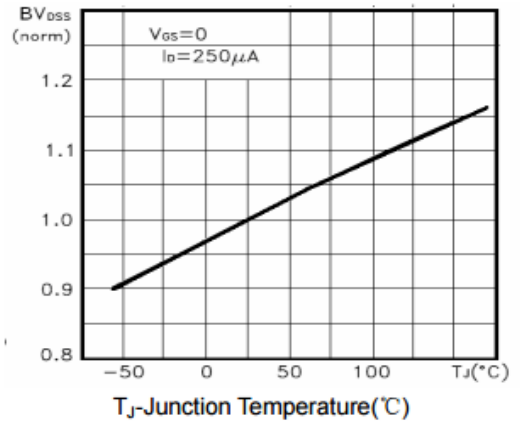


Figure 9 BV_{DSS} vs Junction Temperature

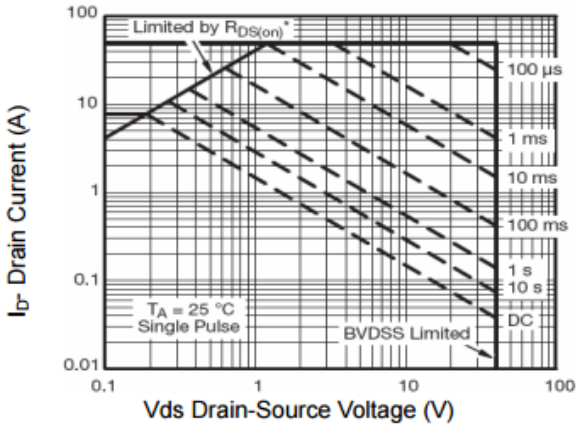


Figure 8 Safe Operation Area

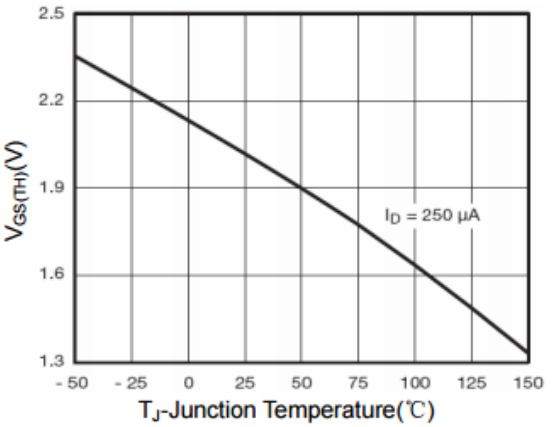


Figure 10 $V_{GS(th)}$ vs Junction Temperature

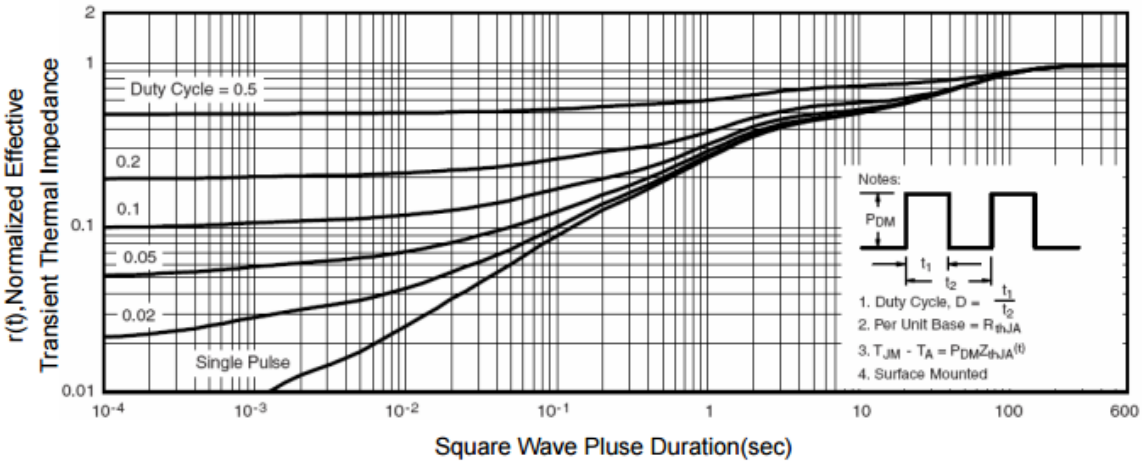


Figure 11 Normalized Maximum Transient Thermal Impedance