RAM Mapping 32x4 LCD Controller for I/O MCU

Features

- Operating voltage: 2.4V ~ 5.2V
- Built-in 256kHz RC oscillator
- External 32.768kHz crystal or 256 kHz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Internal time base frequency sources
- Two selectable buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Built-in time base generator and a WDT
- Time base or WDT overflow output
- 8 kinds of time base/WDT clock sources
- 32x4 LCD driver
- Built-in 32x4 bit display RAM
- 3-wire serial interface
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- R/W address auto increment
- Three data accessing modes
- VLCD pin for adjusting LCD operating voltage
- HT1621B: 48-pin SSOP48/LQFP48 packages
- HT1621B: 44-pin LQFP44 packages
- HT1621D: 28-pin SKDIP28 package
- HT1621G: 48-pad Gold bumped chip

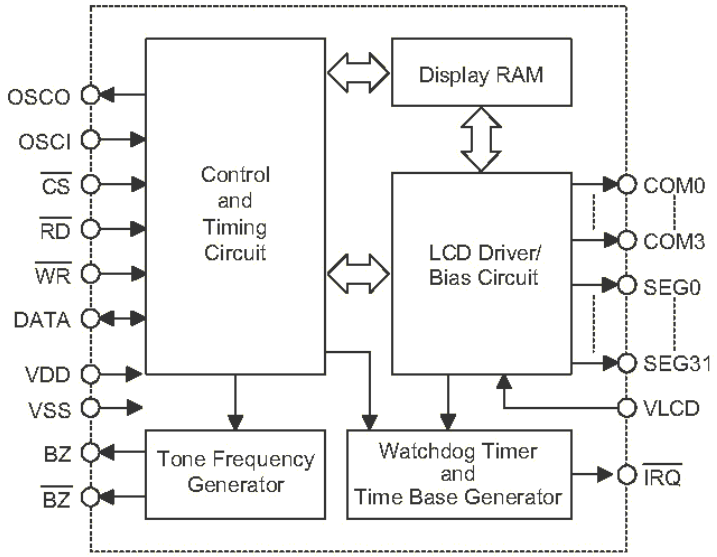
General Description

The HT1621 is a 128 pattern (32x4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the HT1621 makes it suitable for multiple LCD applications including LCD modules and display sub-systems. Only three or four lines are required for the interface between the host controller and the HT1621. The HT1621 contains a power down command to reduce power consumption.

Selection Table

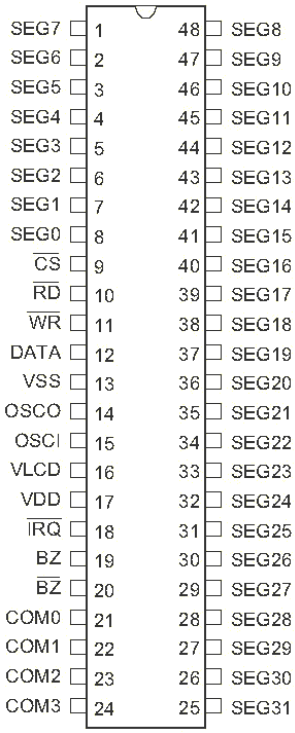
HT162X	HT1620	HT1621	HT1622	HT16220	HT1623	HT1625	HT1626
COM	4	4	8	8	8	8	16
SEG	32	32	32	32	48	64	48
Built-in Osc.	—	√	√	—	√	√	√
Crystal Osc.	√	√	—	√	√	√	√

Block Diagram

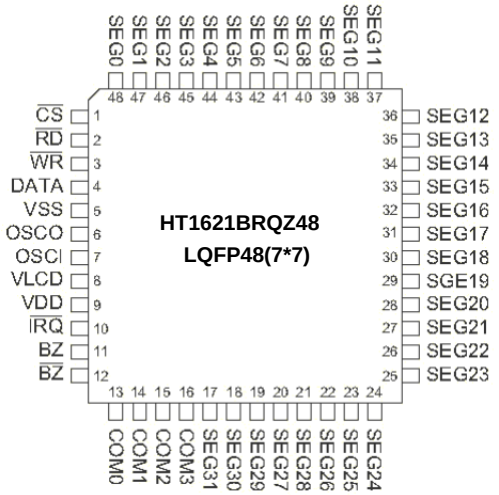


Note: CS:chip selection
BZ, BZ: Tone outputs
WR, RD,DATA: Serial interface
COM0~COM3, SEG0 ~SEG31:LCD outputs
IRQ: Time base or WDT overflow output

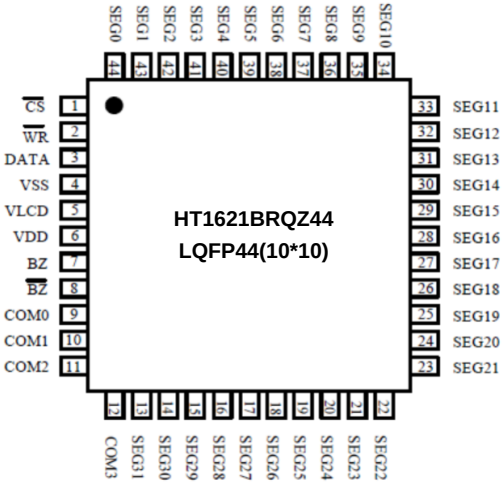
Pin Assignment



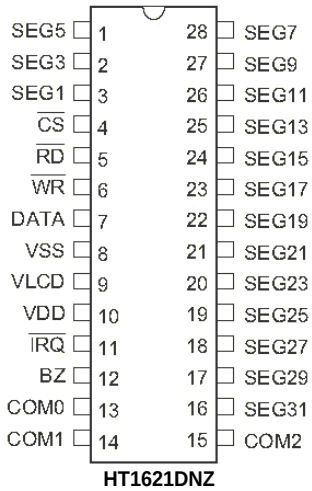
HT1621BRSZ
SSOP48



HT1621BRQZ48
LQFP48(7*7)



HT1621BRQZ44
LQFP44(10*10)



HT1621DNZ
DIP28

Absolute Maximum Ratings

Supply Voltage……V_{SS} –0.3V to V_{SS} +5.5V　　Storage Temperature……-50℃ to 125℃

Input Voltage……V_{SS} –0.3V to V_{DD} +0.3V　　Operating Temperature……-40℃ to 85℃

Note: These are stress ratings only. Stresses exceeding the range specified under " Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics **Ta=25℃**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	—	5.2	V
I_{DD1}	Operating Current	3V	No load/LCD ON	—	150	300	μA
		5V	On-chip RC oscillator	—	300	600	μA
I_{DD2}	Operating Current	3V	No load/LCD ON	—	60	120	μA
		5V	Crystal oscillator	—	120	240	μA
I_{DD3}	Operating Current	3V	No load/LCD ON	—	100	200	μA
		5V	External clock source	—	200	400	μA
I_{STB}	Standby Current	3V	No load, Power down mode	—	0.1	5	μA
		5V		—	0.3	10	μA
V_{IL}	Input Low Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V_{IH}	Input High Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	—	3.0	V
		5V		4.0	—	5.0	V
I_{OL1}	DATA, BZ, $\overline{BZ}$, $\overline{IRQ}$	3V	V_{OL}=0.3V	0.5	1.2	—	mA
		5V	V_{OL}=0.5V	1.3	2.6	—	mA
I_{OH1}	DATA, BZ, $\overline{BZ}$	3V	V_{OH}=2.7V	-0.4	-0.8	—	mA
		5V	V_{OH}=4.5V	-0.9	-1.8	—	mA
I_{OL2}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	150	—	μA
		5V	V_{OL}=0.5V	150	250	—	μA
I_{OH2}	LCD Common Source Current	3V	V_{OH}=2.7V	-80	-120	—	μA
		5V	V_{OH}=4.5V	-120	-200	—	μA
I_{OL3}	LCD Segment Sink Current	3V	V_{OL}=0.3V	60	120	—	μA
		5V	V_{OL}=0.5V	120	200	—	μA
I_{OH3}	LCD Segment Source Current	3V	V_{OH}=2.7V	-40	-70	—	μA
		5V	V_{OH}=4.5V	-70	-100	—	μA
R_{PH}	Pull-high Resistor	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	60	120	200	kΩ
		5V		30	60	100	kΩ

A.C. Characteristics

Ta=25℃

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System clock	—	On-chip RC oscillator	—	256	—	kHz
f_{SYS2}	System clock	—	Crystal oscillator	—	32.768	—	kHz
f_{SYS3}	System clock	—	External clock source	—	256	—	kHz
f_{LCD}	LCD Clock	—	On-chip RC oscillator	—	f_{SYS1}/1024	—	Hz
		—	Crystal oscillator	—	f_{SYS2}/128	—	Hz
		—	External clock source	—	f_{SYS3}/1024	—	Hz
t_{COM}	LCD Common Period	—	n: Number of COM	—	n/ f_{LCD}	—	s
f_{CLK1}	Serial Data Clock ($\overline{WR}$ pin)	3V	Duty cycle 50%	4	—	150	kHz
		5V		4	—	300	kHz
f_{CLK2}	Serial Data Clock ($\overline{RD}$ pin)	3V	Duty cycle 50%	—	—	75	kHz
		5V		—	—	150	kHz
f_{TONE}	Tone Frequency	—	On-chip RC oscillator	—	2.0 or 4.0	—	kHz
t_{CS}	Serial Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	—	250	—	ns
t_{CLK}	$\overline{WR}$,$\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	125	μs
			Read mode	6.67	—	—	
		5V	Write mode	1.67	—	125	μs
			Read mode	3.34	—	—	
t_r, t_f	Rise/Fall Time Serial Data Clock Width (Figure 1)	—	—	—	120	—	ns
t_{au}	Setup Time for DATA to $\overline{WR}$,$\overline{RD}$ Clock Width (Figure 2)	—	—	—	120	—	ns
t_h	Hold Time for DATA to $\overline{WR}$,$\overline{RD}$ Clock Width (Figure 2)	—	—	—	120	—	ns
t_{au1}	Setup Time for $\overline{CS}$ to $\overline{WR}$,$\overline{RD}$ Clock Width (Figure 3)	—	—	—	100	—	ns
t_{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$,$\overline{RD}$ Clock Width (Figure 2)	—	—	—	100	—	ns

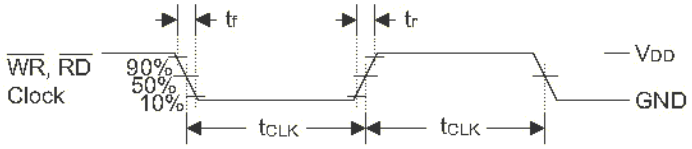


Figure 1

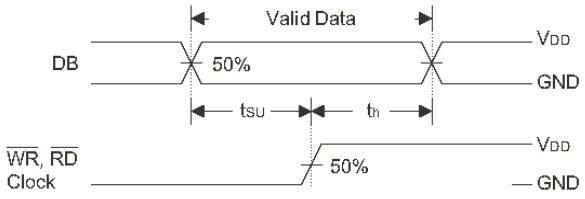


Figure 2

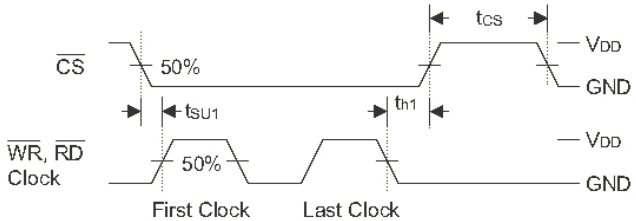
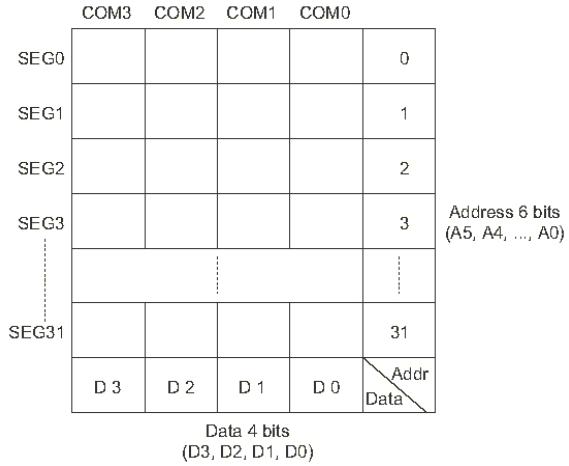


Figure 3

Functional Description

Display Memory –RAM

The static display memory (RAM) is organized into 32x4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY- WRITE commands. The following is a mapping from the RAM to the LCD pattern:



RAM Mapping

System Oscillator

The HT1621 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator (256kHz), a crystal oscillator (32.768kHZ), or an external 256kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is ,however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256kHz clock source operation. At the initial system power on, the HT1621 is at the SYS DIS state.

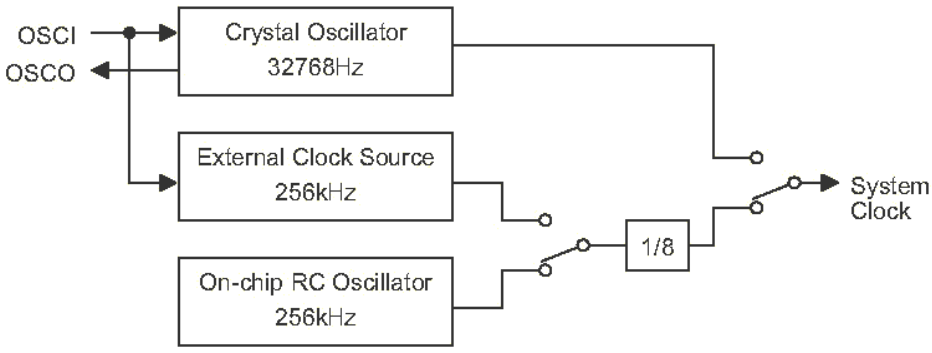
Time Base and Watchdog Timer (WDT)

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT), on the other hand, is composed of an 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the $\overline{IRQ}$ output by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

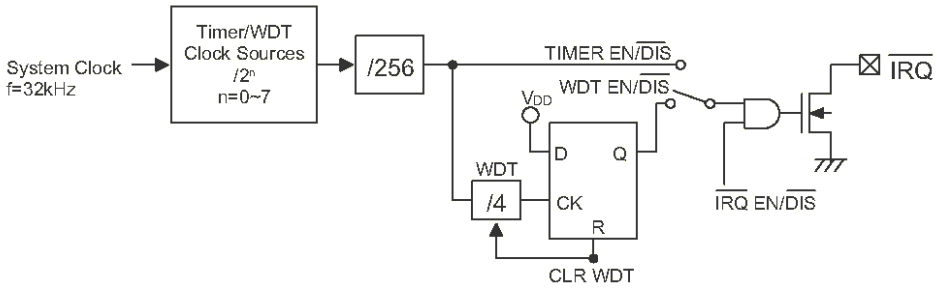
$$f_{WDT} = \frac{32kHz}{2^n}$$

Where the value of n ranges from 0 to 7 by command options. The 32kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768kHz, an on-chip oscillator (256kHz), or an external frequency of 256KHz.

If an on-chip oscillator (256kHz) or an external 256kHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 32kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command not only enables the time base generator but activates



System Oscillator Configuration



Timer and WDT Configurations

The WDT time-out flag output (connect the WDT time-out flag to the $\overline{IRQ}$ pin). After the TIMER EN command is transferred, the WDT is disconnected from the $\overline{IRQ}$ pin, and the output of the time base generator is connected to the $\overline{IRQ}$ pin. The WDT can be cleared by executing the CLR WDT command, and the contents of the time base generator is cleared by executing the CLR WDT or the CLR TIMER command. The CLR WDT or the CLR TIMER command should be executed prior to the WDT EN or the TIMER EN command respectively. Before executing the $\overline{IRQ}$ EN command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will stay at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued. After the $\overline{IRQ}$ output is disabled the $\overline{IRQ}$ pin will remain at the floating state. The $\overline{IRQ}$ output can be enabled or disabled by executing the $\overline{IRQ}$ EN or the $\overline{IRQ}$ DIS command, respectively. The $\overline{IRQ}$ EN makes the output of the time base generator or of the WDT time-out flag appear on the $\overline{IRQ}$ pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions.

On the other hand if an external clock is selected as the source of system frequency the SYS DIS command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the HT1621 will continue working until system power fails or the external clock source is removed. After the system power on, the $\overline{IRQ}$ will be disabled.

Tone Output

A simple tone generator is implemented in the HT1621.The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$, which are used to generate a single tone. By executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable. The TONE4K and TONE2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned on or off by invoking the TONE ON or the TONE OFF command. The tone outputs , namely BZ and $\overline{BZ}$, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{BZ}$ outputs will remain at low level.

LCD Driver

The HT1621 is a 128 (32x4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the HT1621 suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 32.768kHz crystal oscillator frequency, an on-chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table.

The bold form of 100, namely 100, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command, will be omitted. The LCD OFF command turns the LCD display off by disabling the LCD bias generator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS and COM are the LCD panel related commands. Using the LCD related commands, the HT1621 can be compatible with most types of LCD panels.

Name	Command Code	Function
LCD OFF	10000000010X	Turn off LCD outputs
LCD ON	10000000011X	Turn on LCD outputs
BIAS & COM	1000010abxcx	C=0:1/2 bias option C=1: 1/3 bias option ab=00:2 commons option ab=01:3 commons option ab=10:4 commons option

Command Format

The HT1621 can be configured by the S/W setting . There are two mode commands to configure the HT1621 resources and to transfer the LCD display data. The configuration mode of the HT1621 is called command mode, and its command mode ID is 100. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDS and the command mode ID;

Operation	Mode	ID
Read	Data	110
Write	Data	101
Read-Modify-write	Data	101
Command	Command	100

The mode command should be issued before the data or command is transferred. If successive commands have been issued. The command mode ID, namely 100, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will be reset also. Once the $\overline{CS}$ pin returns to "0" a new operation mode ID should be issued first.

Interfacing

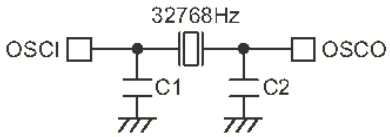
Only four lines are required to interface with the HT1621, the $\overline{CS}$ line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the HT1621. If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the HT1621 are first disabled and then initialized.

Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the HT1621. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The $\overline{RD}$ line is the READ clock input Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal. The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the HT1621 on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the HT1621. The $\overline{IRQ}$ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the $\overline{IRQ}$ pin of the HT1621.

Crystal Selection

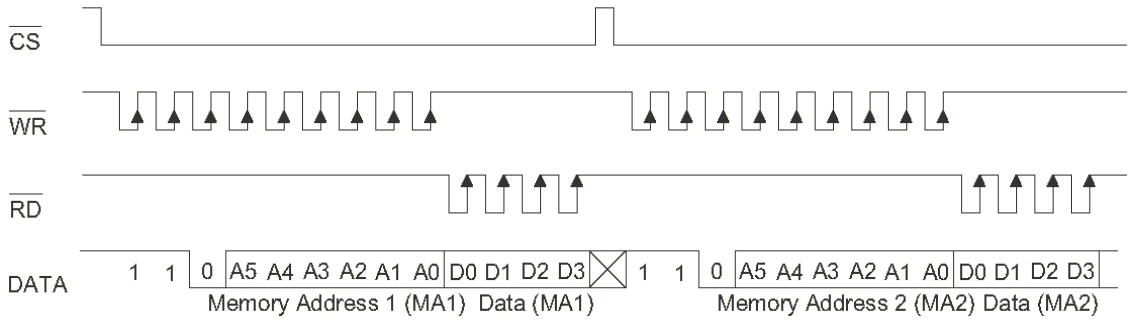
A 32768Hz crystal can be directly connected to the HT1621 via OSCI and OSCO. In order to obtain the correct frequency, two additional load capacities (C1, C2) are needed. The value of the capacity depends on how accurate the crystal is. We suggest that you can follow the table. Which suggests the value of capacities. The table illustrations the suggestion value of capacities (C1, C2)

Crystal Error	Capacity Value
±10ppm	0~10p
10~20ppm	10~20p

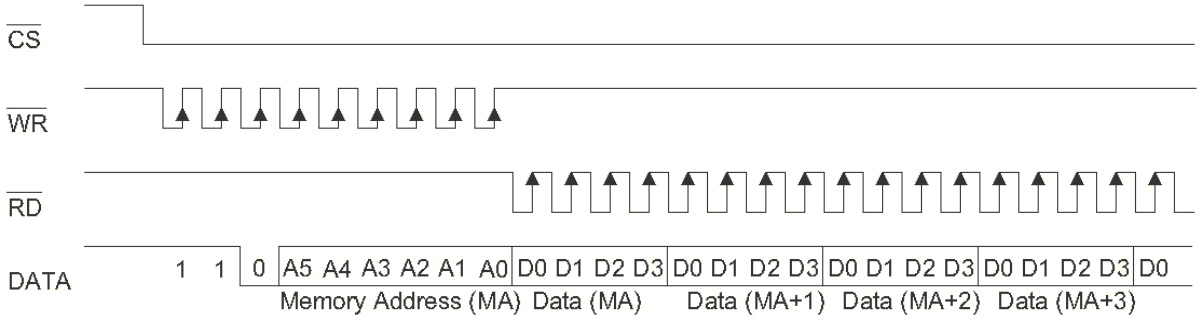


Timing Diagrams

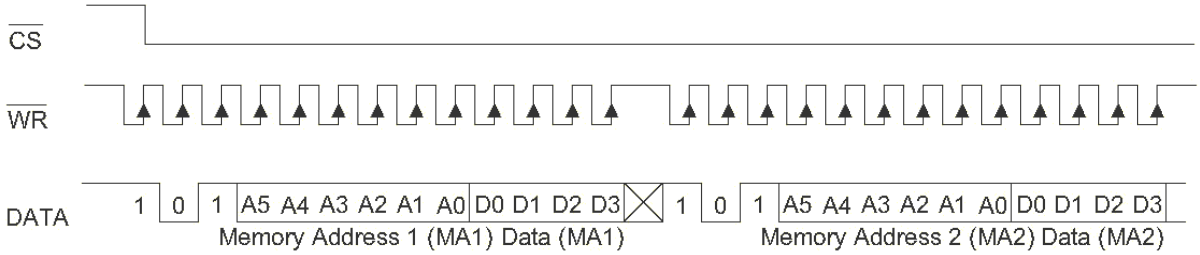
READ Mode (Command Code:110)



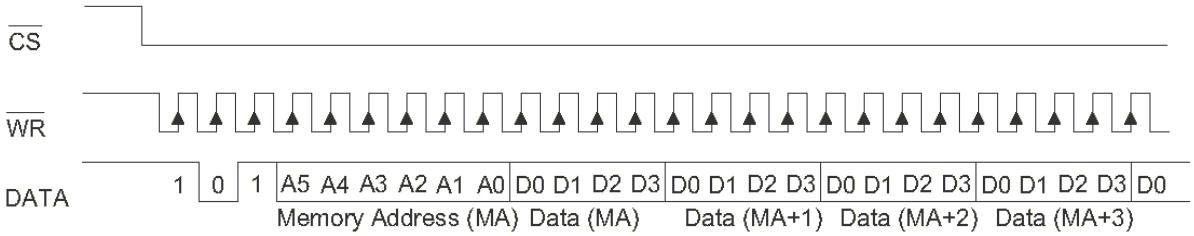
READ Mode (Successive Address Reading)



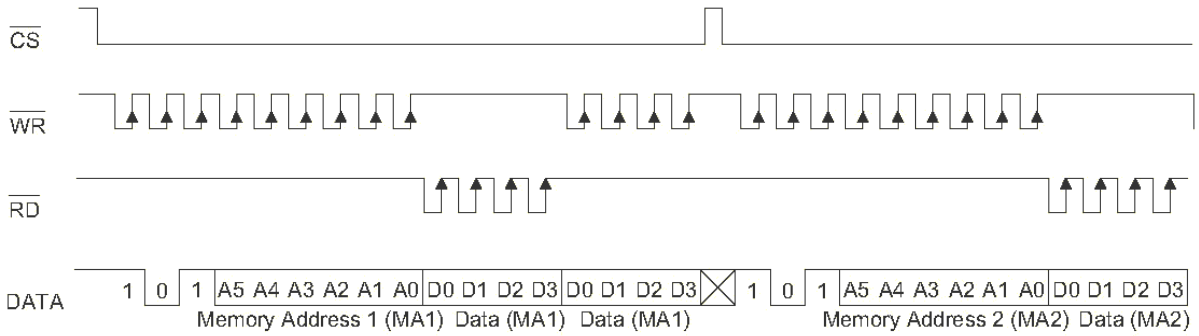
WRITE Mode (Command Code: 101)



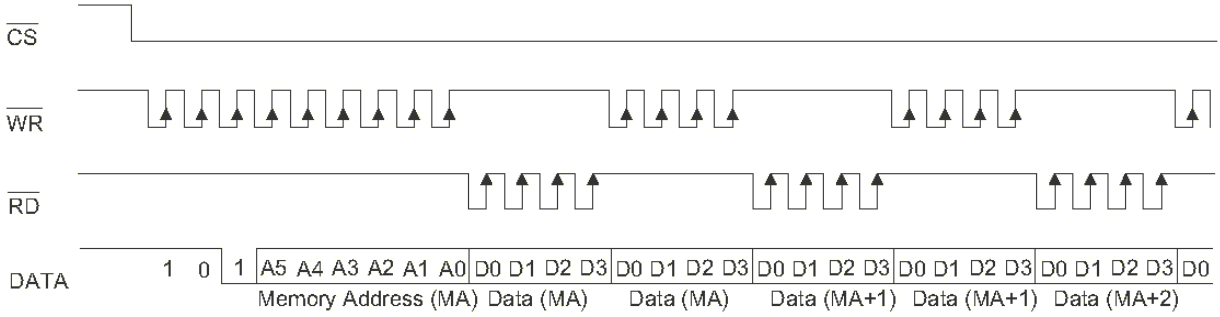
Write Mode (Successive Address Writing)



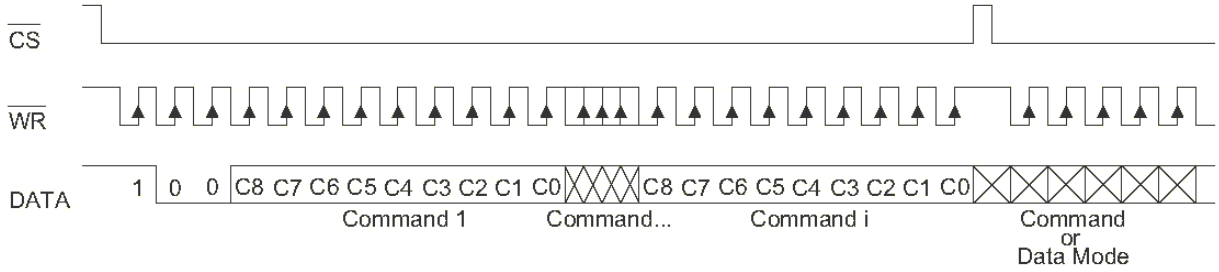
Read-Modify-Write Mode (Command Code: 101)



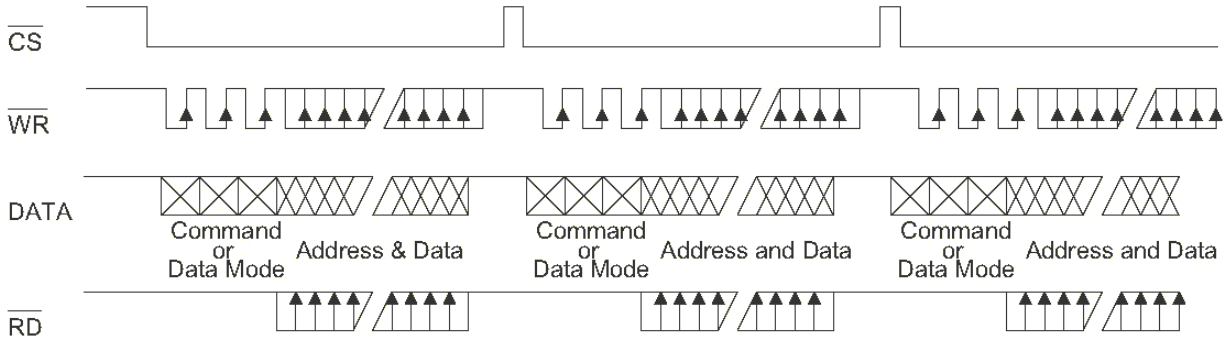
Read-Modify-Write Mode (Successive Address Accessing)



Command Mode (Command Code : 100)



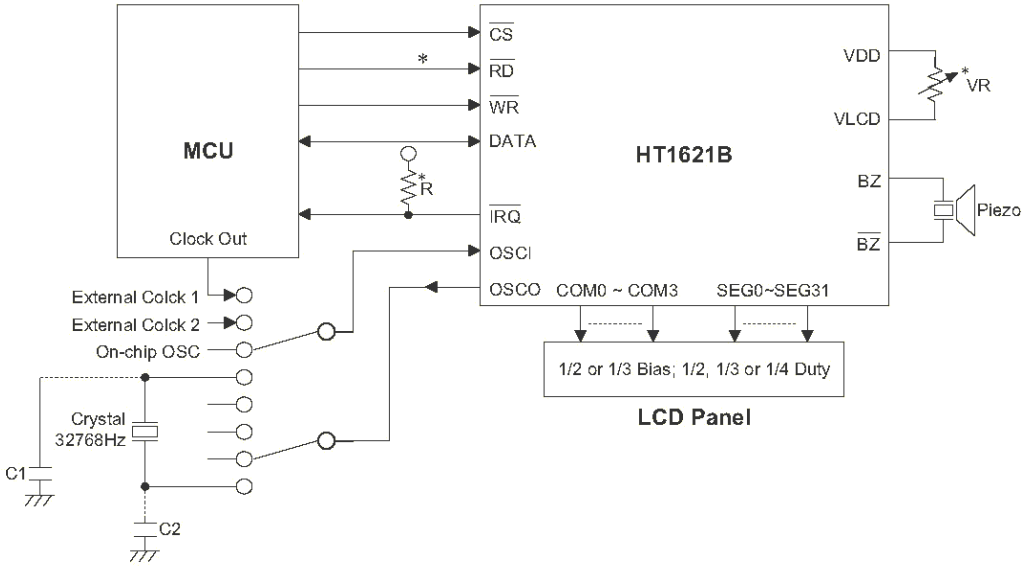
Mode (Data and Command Mode)



Note: It is recommended that the host controller should read in the data from the DATA line between the rising edge of the $\overline{RD}$ line and the falling edge of the next $\overline{RD}$ line.

Application Circuits

Host Controller with an HT1621 Display System



Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the requirement of the MCU.

The voltage applied to V_{LCD} pin must be lower than V_{DD}.

Adjust VR to fit LCD display, at V_{DD} = 5V, V_{LCD} = 4V, VR=15kΩ ± 20%.

Adjust R (external pull-high resistance) to fit user's time base clock.

In order to obtain the correct frequency, two additional load capacities (C1,C2) are needed. The value of the capacity depends on how accurate the crystal is. We suggest that you can follow the table, which suggests the value of capacities.

The table illustrations the suggestion value of capacities (C1,C2)

Crystal Error	Capacity Value
±10ppm	0~10p
10~20ppm	10~20p

Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off both system oscillator and LCD Bias generator	Yes
SYS EN	100	0000-0001-X	C	Turn on system oscillator	
LCD OFF	100	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	100	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	100	0000-0100-X	C	Disable time base output	
WDT DIS	100	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	100	0000-0110-X	C	Enable time base output	
WDT EN	100	0000-0111-X	C	Enable WDT time-out flag output	

Name	ID	Command Code	D/C	Function	Def.
TONE OFF	100	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	100	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	100	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	100	0000-111X-X	C	Clear the contents of WDT stage	
XTAL 32K	100	0001-01XX-X	C	System clock source, crystal oscillator	
RC 256K	100	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes
EXT 256K	100	0001-11XX-X	C	System clock source, external clock source	
BIAS 1/2	100	0010-abX0-X	C	LCD 1/2 bias option ab=00:2 commons option ab=01:3 commons option ab=10:4 commons option	
BIAS 1/3	100	0010-abX1-X	C	LCD 1/3 bias option ab=00:2 commons option ab=01:3 commons option ab=10:4 commons option	
TONE 4K	100	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2K	100	011X-XXXX-X	C	Tone frequency, 2kHz	
$\overline{\text{IRQ}}$DIS	100	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	Yes
$\overline{\text{IRQ}}$EN	100	010X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	
F1	100	101X-X000-X	C	Time base/WDT clock output: 1Hz The WDT time-out flag after: 4s	
F2	100	101X-X001-X	C	Time base/WDT clock output: 2Hz The WDT time-out flag after: 2s	
F4	100	101X-X010-X	C	Time base/WDT clock output: 4Hz The WDT time-out flag after: 1s	
F8	100	101X-X011-X	C	Time base/WDT clock output: 8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-X100-X	C	Time base/WDT clock output: 16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-X101-X	C	Time base/WDT clock output: 32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-X110-X	C	Time base/WDT clock output: 64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-X111-X	C	Time base/WDT clock output: 128Hz The WDT time-out flag after: 1/32s	Yes
TEST	100	1110-0000-X	C	Test mode, user don't use.	
NORMAL	100	1110-0011-X	C	Normal mode	Yes

Note: x: Don't care

A5~A0:RAM addresses

D3~D0: RAM data

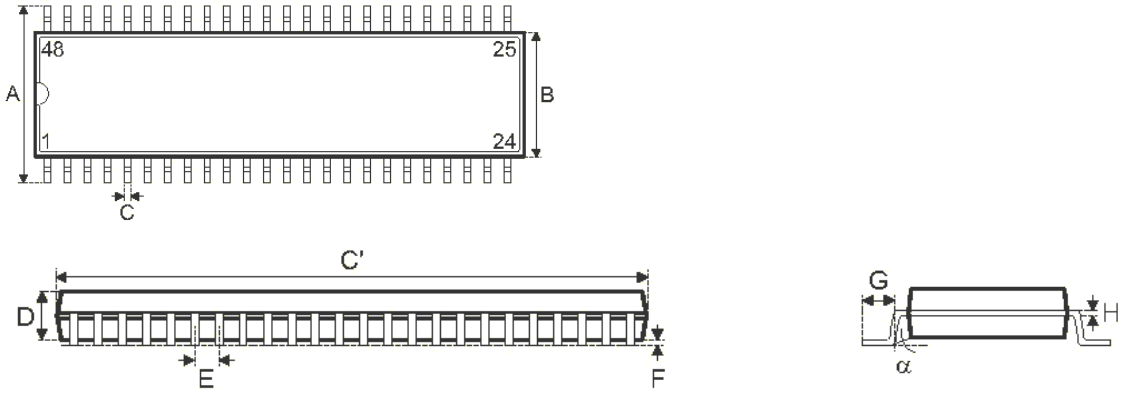
D/C: Data/command mode

Def.: Power on reset default

All the bold forms, namely 110,101, and 100, are mode commands, of these, 100 indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on-chip 256kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 256kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1621 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the HT1621.

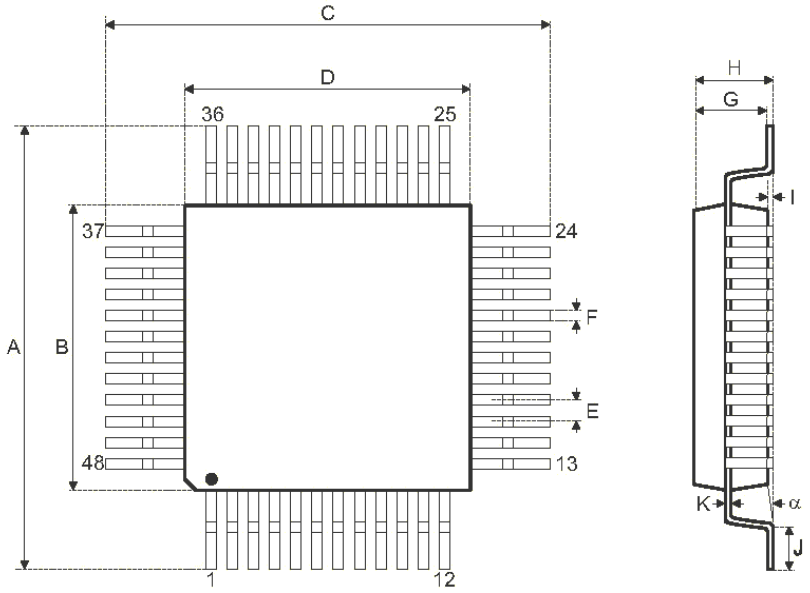
Package Information

48-pin SSOP (300mil) Outline Dimensions



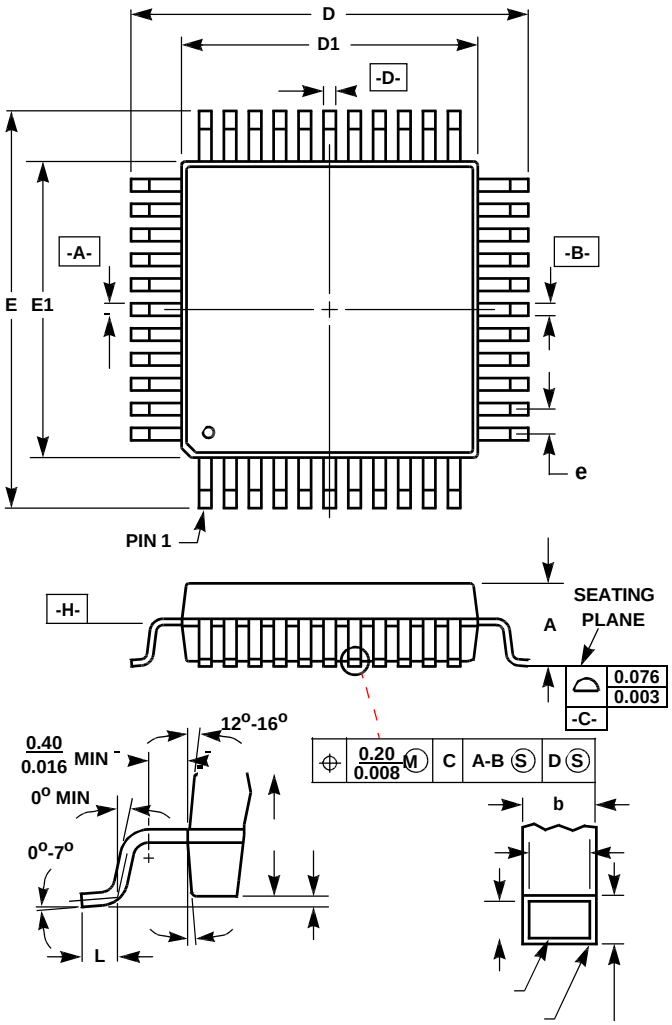
Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	395	—	420
B	291	—	299
C	8	—	12
C'	613	—	637
D	85	—	99
E	—	25	—
F	4	—	10
G	25	—	35
H	4	—	12
α	0°	—	8°

48-pin LQFP (7x7) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.50	—
F	—	0.20	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°

44-pin LQFP (10x10) Outline Dimensions



Q44.10x10 (JEDEC MS-022AB ISSUE B)
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SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.096	-	2.45	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
b	0.012	0.018	0.30	0.45	6
b1	0.012	0.016	0.30	0.40	-
D	0.515	0.524	13.08	13.32	3
D1	0.389	0.399	9.88	10.12	4, 5
E	0.516	0.523	13.10	13.30	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.026	0.029	0.65	0.75	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

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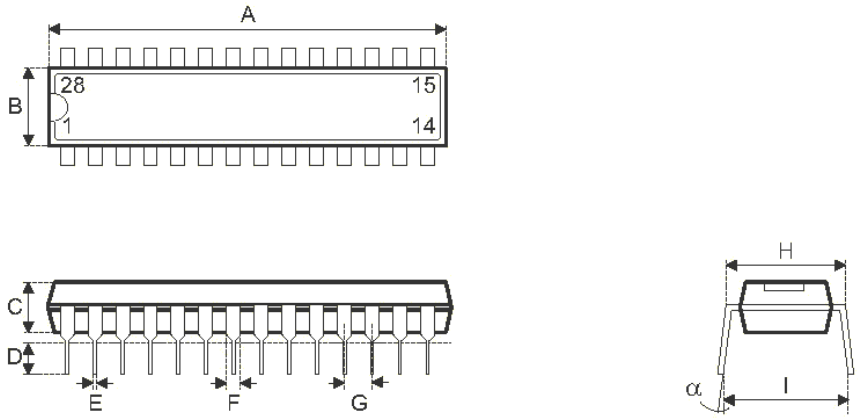
28-pin SKDIP (300mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	1375	—	1395
B	278	—	298
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	330	—	375
α	0°	—	15°