NCP161

450 mA, Ultra-Low Noise and High PSRR LDO Regulator for RF and Analog Circuits

The NCP161 is a linear regulator capable of supplying 450 mA output current. Designed to meet the requirements of RF and analog circuits, the NCP161 device provides low noise, high PSRR, low quiescent current, and very good load/line transients. The device is designed to work with a 1 μF input and a 1 μF output ceramic capacitor. It is available in two thickness ultra−small 0.35P, 0.65 mm x 0.65 mm Chip Scale Package (CSP) and XDFN4 0.65P, 1 mm x 1 mm.

Features

- Operating Input Voltage Range: 1.9 V to 5.5 V
- Available in Fixed Voltage Option: 1.8 V to 5.14 V
- ±2% Accuracy Over Load/Temperature
- Ultra Low Quiescent Current Typ. 18 μA
- Standby Current: Typ. 0.1 μA
- Very Low Dropout: 150 mV at 450 mA
- Ultra High PSRR: Typ. 98 dB at 20 mA, f = 1 kHz
- Ultra Low Noise: 10 μV_{RMS}
- Stable with a 1 μF Small Case Size Ceramic Capacitors
- Available in −WLCSP4 0.65 mm x 0.65 mm x 0.4 mm
  −WLCSP4 0.65 mm x 0.65 mm x 0.33 mm
  −XDFN4 1 mm x 1 mm x 0.4 mm
  −SOT23−5 2.9 mm x 2.8 mm x 1.2 mm
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery−powered Equipment
- Wireless LAN Devices
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

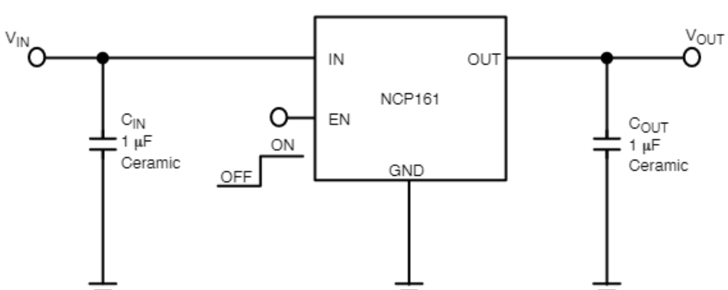

Figure 1. Typical Application Schematics

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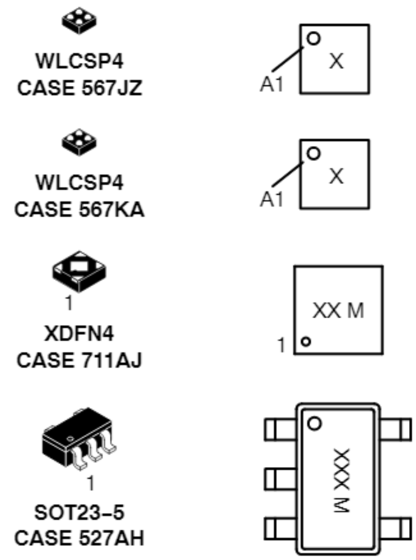
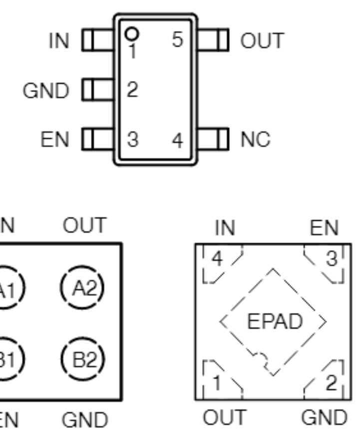
MARKING DIAGRAMS



X, XX, XXX = Specific Device Code
M = Date Code

PIN CONNECTIONS (Top Views)



ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

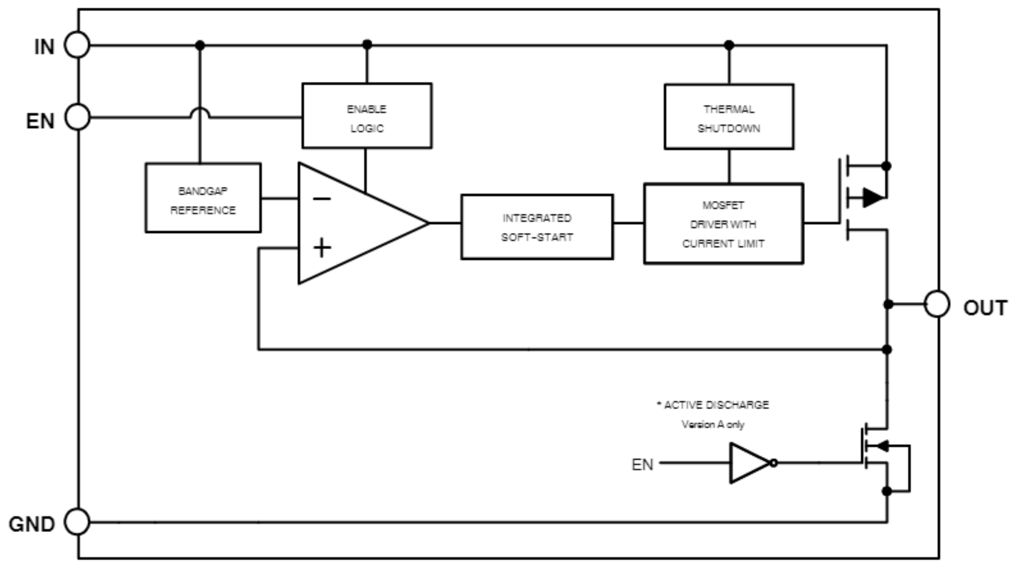


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. CSP4	Pin No. SOT23−5	Pin No. XDFN4	Pin Name	Description
A1	1	4	IN	Input voltage supply pin
A2	5	1	OUT	Regulated output voltage. The output should be bypassed with small 1 μF ceramic capacitor.
B1	3	3	EN	Chip enable: Applying V_{EN} < 0.4 V disables the regulator, Pulling V_{EN} > 1.2 V enables the LDO.
B2	2	2	GND	Common ground connection
–	–	EPAD	EPAD	Expose pad should be tied to ground plane for better power dissipation

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3, max. 6	V
Chip Enable Input	V_{CE}	−0.3 to 6	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating		Symbol	Value	Unit
Thermal Characteristics, CSP4 (Note 3)	Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	108	°C/W
Thermal Characteristics, XDFN4 (Note 3)	Thermal Resistance, Junction−to−Air		198.1	
Thermal Characteristics, SOT23−5 (Note 3)	Thermal Resistance, Junction−to−Air		218	

3. Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7

ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 125°C$; $V_{IN} = V_{OUT(NOM)} + 1$ V; $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1$ μF, unless otherwise noted. $V_{EN} = 1.2$ V. Typical values are at $T_J = +25°C$ (Note 4).

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.9		5.5	V
Output Voltage Accuracy	$V_{IN} = V_{OUT(NOM)} + 1$ V 0 mA ≤ I_{OUT} ≤ 450 mA	WLCSP4, XDFN4	V_{OUT}	−2		+2	%
	$V_{IN} = V_{OUT(NOM)} + 1$ V	SOT23−5		−2		+2	
Line Regulation	$V_{OUT(NOM)} + 1$ V ≤ V_{IN} ≤ 5.5 V		$Line_{Reg}$		0.02		%/V
Load Regulation	I_{OUT} = 1 mA to 450 mA WLCSP4, XDFN4	WLCSP4, XDFN4	$Load_{Reg}$		0.001		%/mA
		SOT23−5			0.005	0.008	
Dropout Voltage (Note 5)	I_{OUT} = 450 mA WLCSP4, XDFN4	$V_{OUT(NOM)}$ = 1.8 V	V_{DO}		300	450	mV
		$V_{OUT(NOM)}$ = 2.5 V			190	315	
		$V_{OUT(NOM)}$ = 2.8 V			175	290	
		$V_{OUT(NOM)}$ = 2.85 V			170	290	
		$V_{OUT(NOM)}$ = 3.0 V			165	275	
		$V_{OUT(NOM)}$ = 3.3 V			160	260	
		$V_{OUT(NOM)}$ = 3.5 V			150	255	
		$V_{OUT(NOM)}$ = 4.5 V			120	210	
		$V_{OUT(NOM)}$ = 5.0 V			105	190	
		$V_{OUT(NOM)}$ = 5.14 V			105	185	
Dropout Voltage (Note 5)	I_{OUT} = 450 mA SOT23−5	$V_{OUT(NOM)}$ = 1.8 V	V_{DO}		365	480	mV
		$V_{OUT(NOM)}$ = 2.8 V			260	345	
		$V_{OUT(NOM)}$ = 3.0 V			240	330	
		$V_{OUT(NOM)}$ = 3.3 V			225	305	
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$		I_{CL}	450	700		mA
Short Circuit Current	V_{OUT} = 0 V		I_{SC}		690		
Quiescent Current	I_{OUT} = 0 mA		I_Q		18	23	μA
Shutdown Current	V_{EN} ≤ 0.4 V, V_{IN} = 4.8 V		I_{DIS}		0.01	1	μA
EN Pin Threshold Voltage	EN Input Voltage “H”		V_{ENH}	1.2			V
	EN Input Voltage “L”		V_{ENL}			0.4	
EN Pull Down Current	V_{EN} = 4.8 V		I_{EN}		0.2	0.5	μA
Turn−On Time	C_{OUT} = 1 μF, From assertion of V_{EN} to V_{OUT} = 95% $V_{OUT(NOM)}$				120		μs
Power Supply Rejection Ratio	I_{OUT} = 20 mA	f = 100 Hz f = 1 kHz f = 10 kHz f = 100 kHz	PSRR		91 98 82 48		dB
Output Voltage Noise	f = 10 Hz to 100 kHz	I_{OUT} = 1 mA I_{OUT} = 250 mA	V_N		14 10		$μV_{RMS}$
Thermal Shutdown Threshold	Temperature rising		T_{SDH}		160		°C
	Temperature falling		T_{SDL}		140		°C
Active output discharge resistance	V_{EN} < 0.4 V, Version A only		R_{DIS}		280		Ω
Line transient (Note 6)	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 1.6 V) in 30 μs, I_{OUT} = 1 mA		$Tran_{LINE}$	−1			mV
	V_{IN} = ($V_{OUT(NOM)}$ + 1.6 V) to ($V_{OUT(NOM)}$ + 1 V) in 30 μs, I_{OUT} = 1 mA					+1	
Load transient (Note 6)	I_{OUT} = 1 mA to 450 mA in 10 μs		$Tran_{LOAD}$	−40			mV
	I_{OUT} = 450 mA to 1mA in 10 μs					+40	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25°C$. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 100 mV below $V_{OUT(NOM)}$.
6. Guaranteed by design.

TYPICAL CHARACTERISTICS

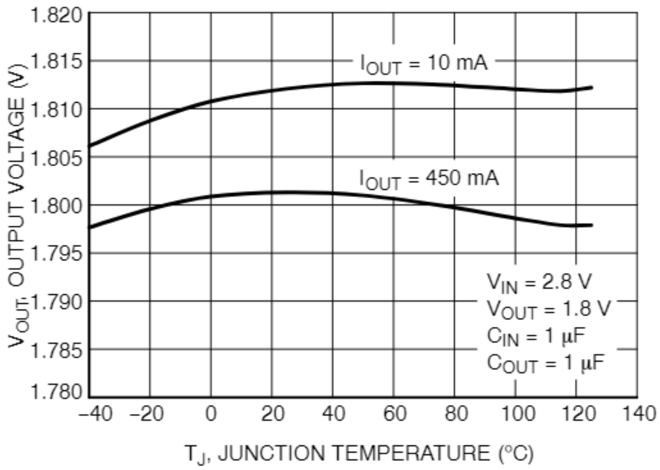


Figure 3. Output Voltage vs. Temperature – V_{OUT} = 1.8 V – XDFN Package

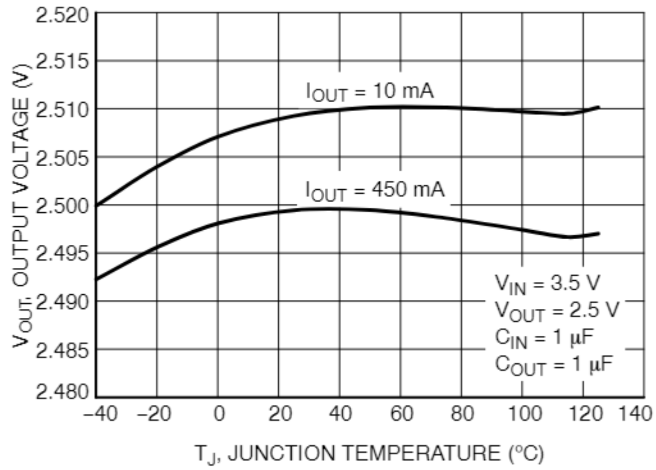


Figure 4. Output Voltage vs. Temperature – V_{OUT} = 2.5 V – XDFN Package

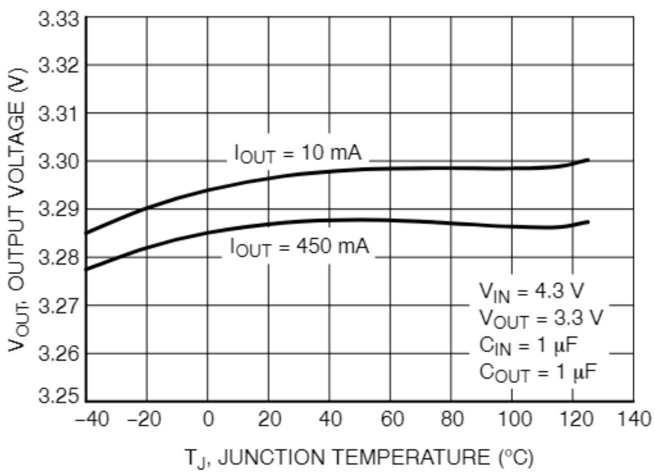


Figure 5. Output Voltage vs. Temperature – V_{OUT} = 3.3 V – XDFN Package

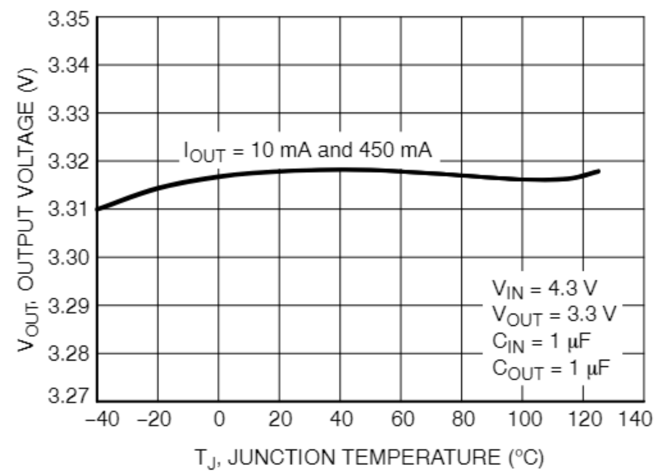


Figure 6. Output Voltage vs. Temperature – V_{OUT} = 3.3 V – CSP Package

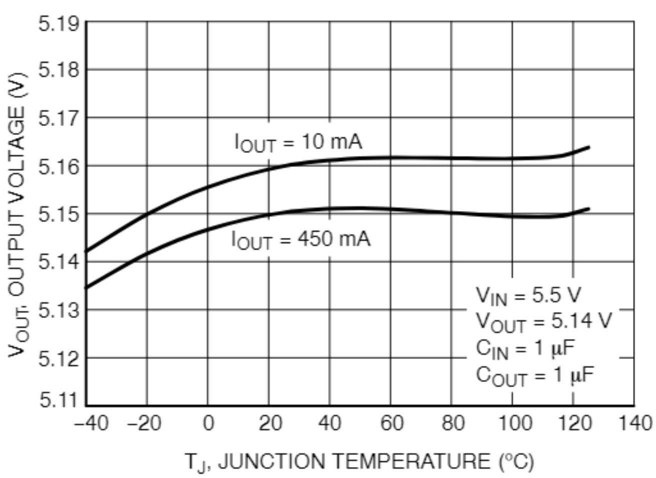


Figure 7. Output Voltage vs. Temperature – V_{OUT} = 5.14 V – XDFN Package

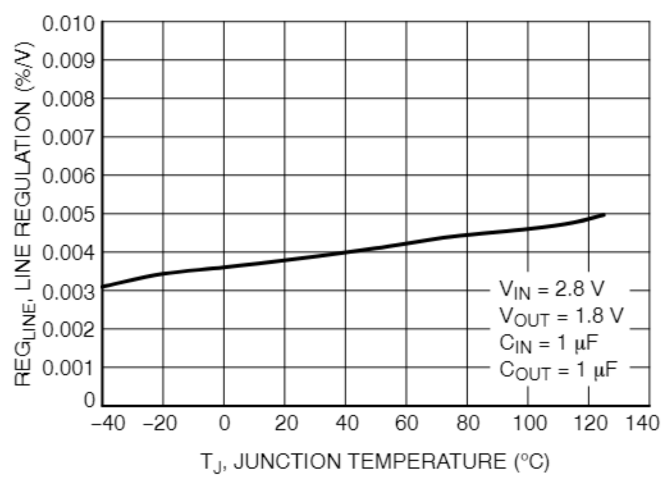


Figure 8. Line Regulation vs. Temperature – V_{OUT} = 1.8 V

TYPICAL CHARACTERISTICS

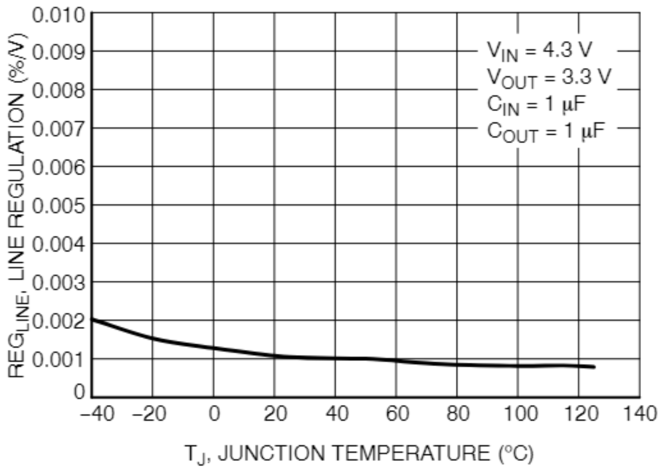


Figure 9. Line Regulation vs. Temperature – V_{OUT} = 3.3 V

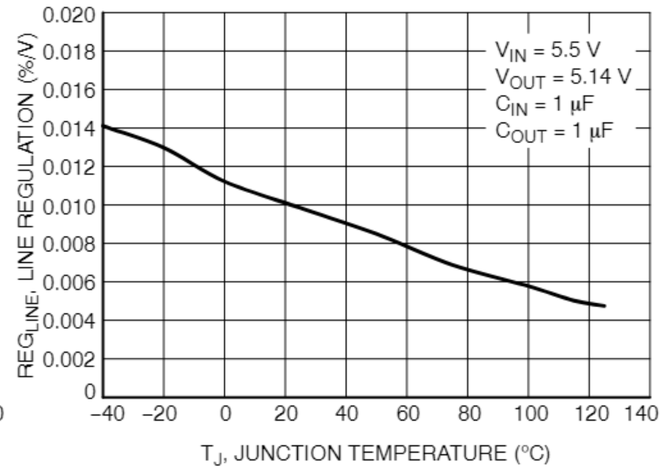


Figure 10. Line Regulation vs. Temperature – V_{OUT} = 5.14 V

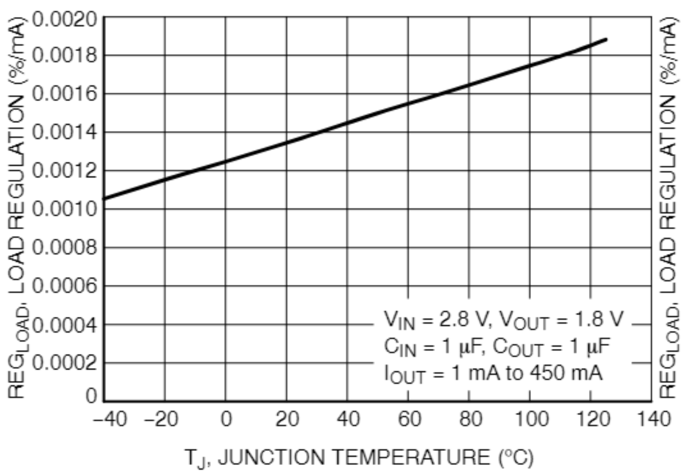


Figure 11. Load Regulation vs. Temperature – V_{OUT} = 1.8 V (WLCSP4)

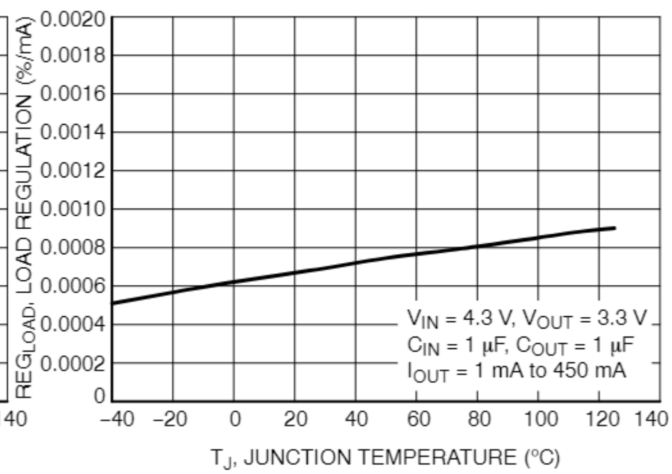


Figure 12. Load Regulation vs. Temperature – V_{OUT} = 3.3 V (WLCSP4)

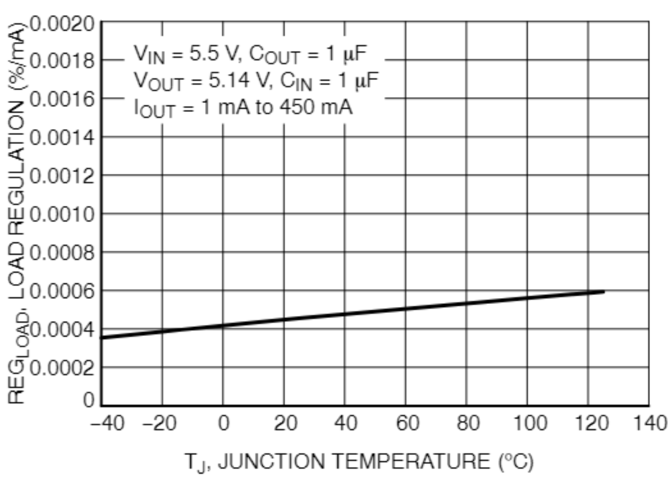


Figure 13. Load Regulation vs. Temperature – V_{OUT} = 5.14 V (WLCSP4)

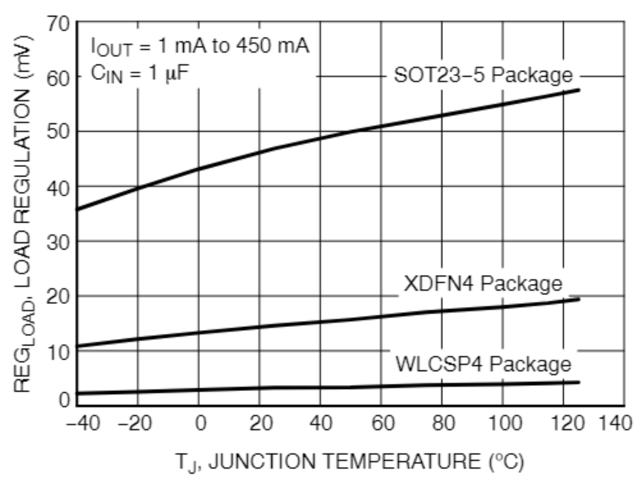


Figure 14. Load Regulation vs. Temperature

TYPICAL CHARACTERISTICS

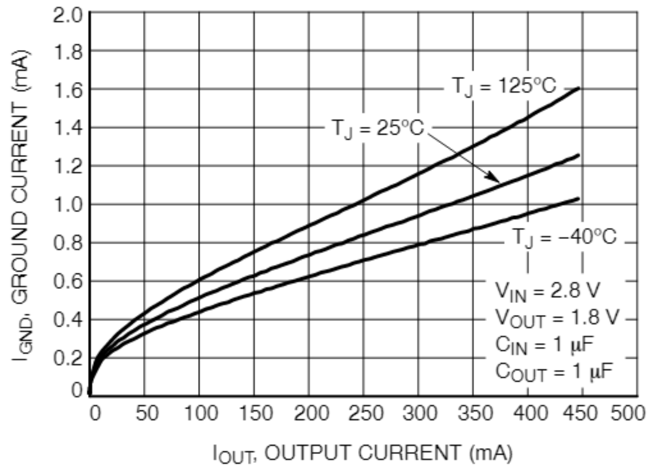


Figure 15. Ground Current vs. Load Current – V_{OUT} = 1.8 V

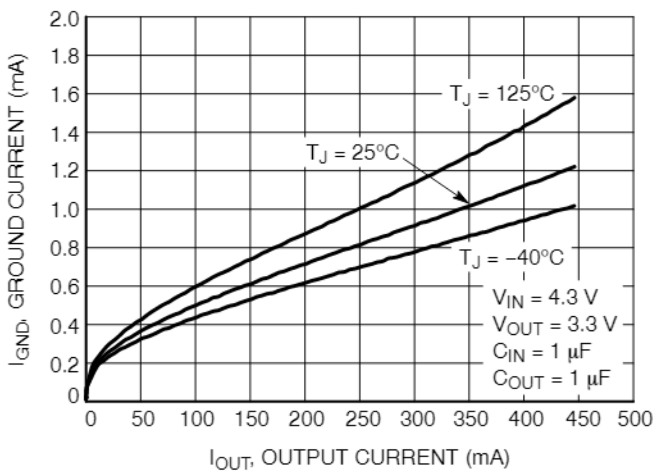


Figure 16. Ground Current vs. Load Current – V_{OUT} = 3.3 V

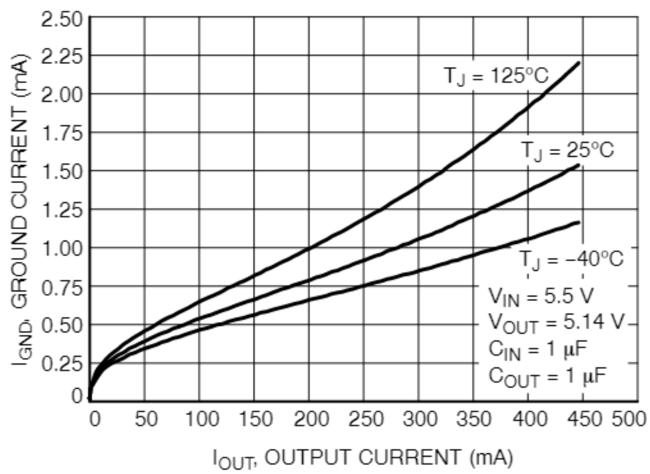


Figure 17. Ground Current vs. Load Current – V_{OUT} = 5.14 V

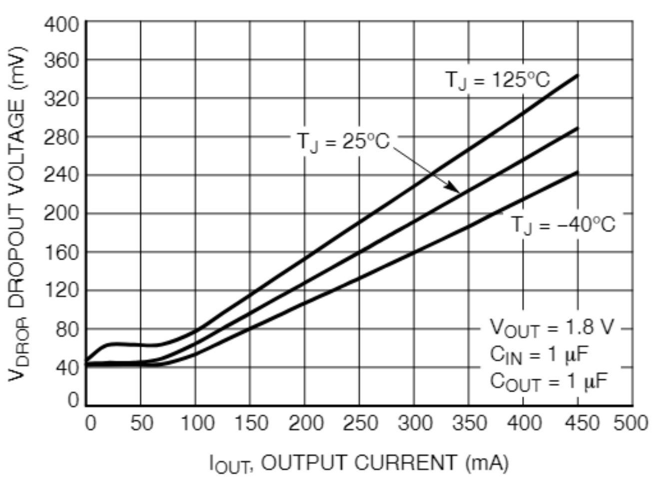


Figure 18. Dropout Voltage vs. Load Current – V_{OUT} = 1.8 V

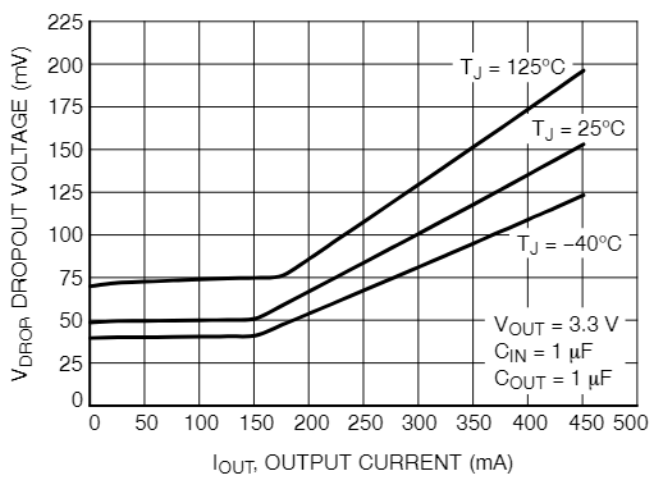


Figure 19. Dropout Voltage vs. Load Current – V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS

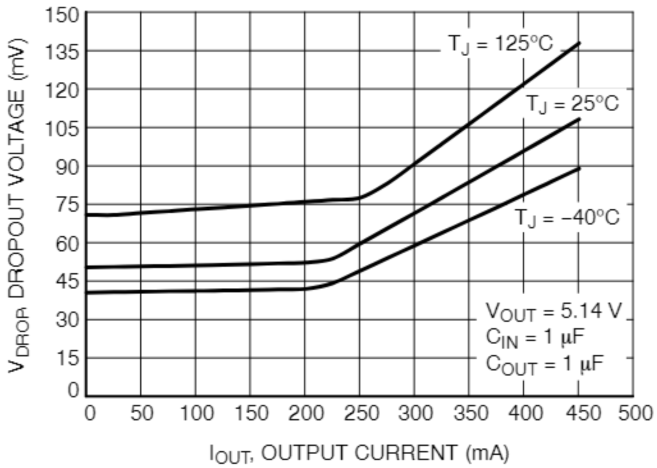


Figure 20. Dropout Voltage vs. Load Current – V_{OUT} = 5.14 V

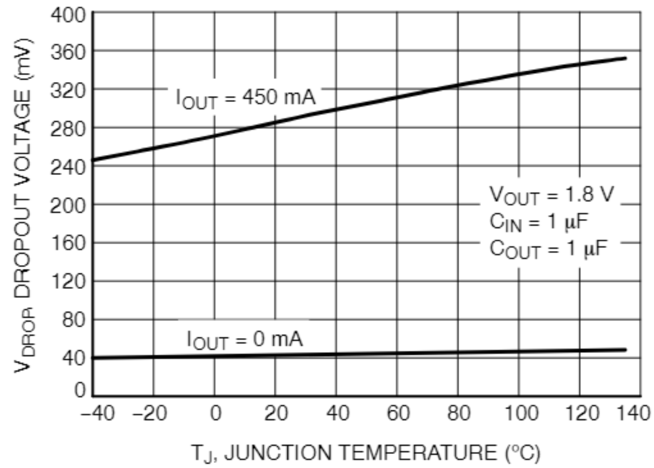


Figure 21. Dropout Voltage vs. Temperature– V_{OUT} = 1.8 V

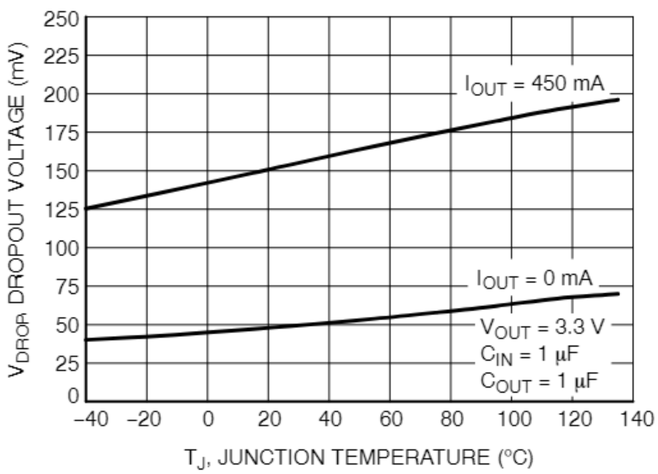


Figure 22. Dropout Voltage vs. Temperature– V_{OUT} = 3.3 V

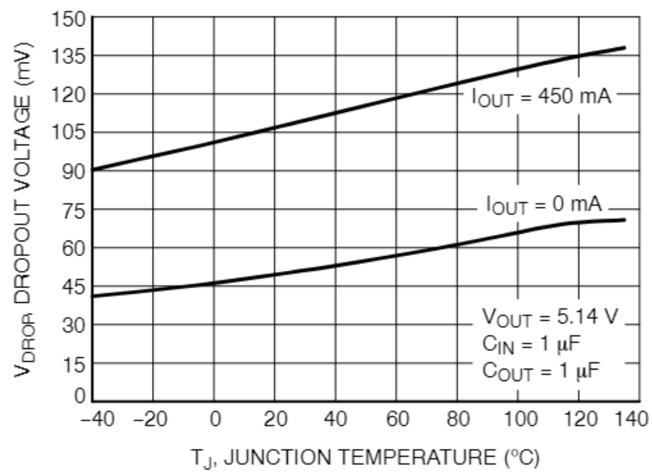


Figure 23. Dropout Voltage vs. Temperature– V_{OUT} = 5.14 V

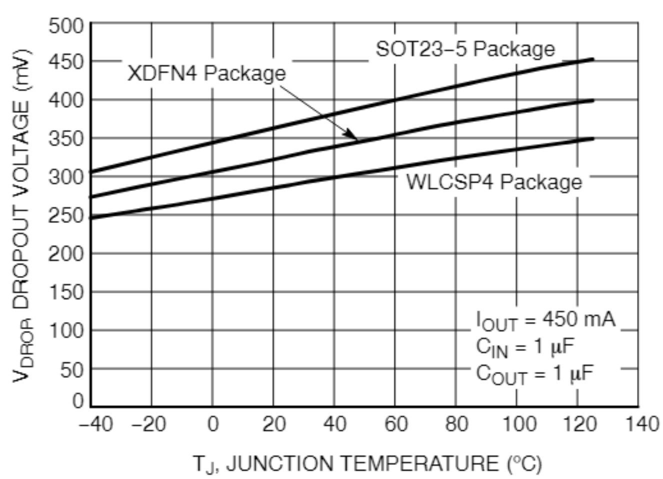


Figure 24. Dropout Voltage vs. Temperature V_{OUT} = 1.8 V

TYPICAL CHARACTERISTICS

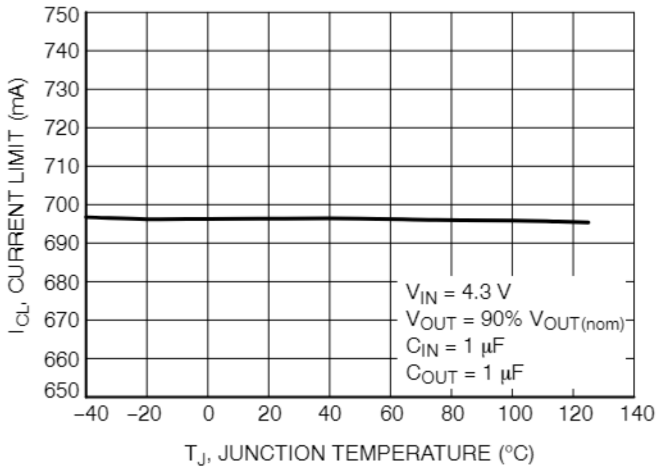


Figure 25. Current Limit vs. Temperature

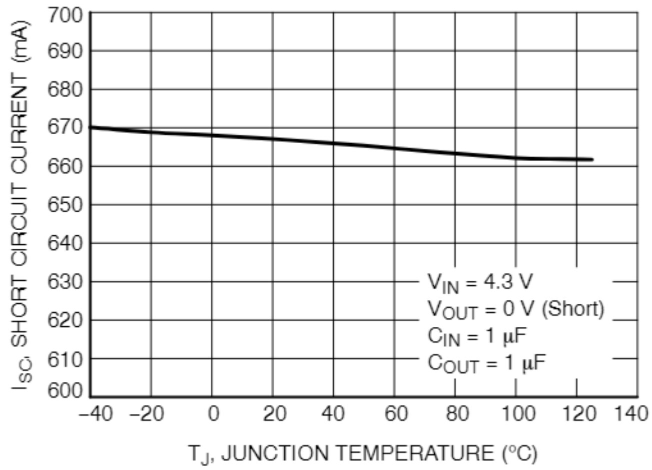


Figure 26. Short Circuit Current vs. Temperature

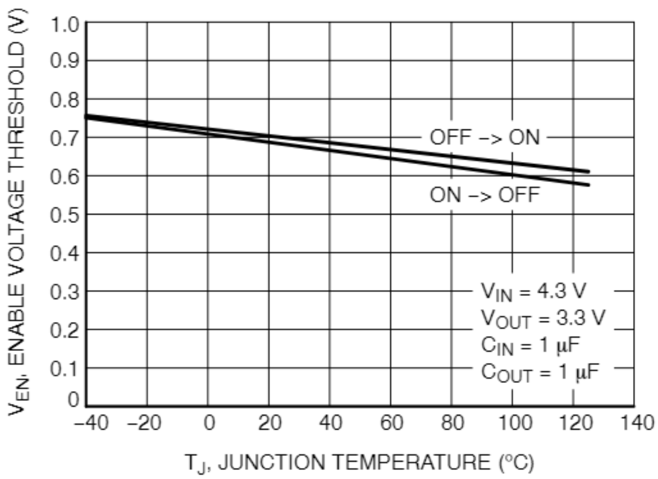


Figure 27. Enable Threshold Voltage vs. Temperature

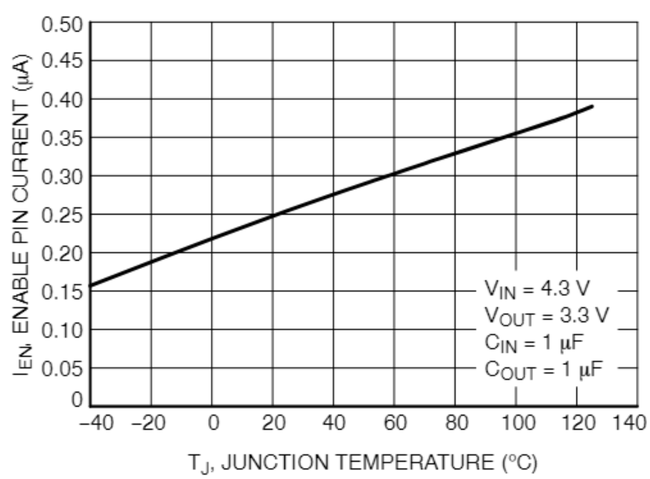


Figure 28. Enable Current Temperature

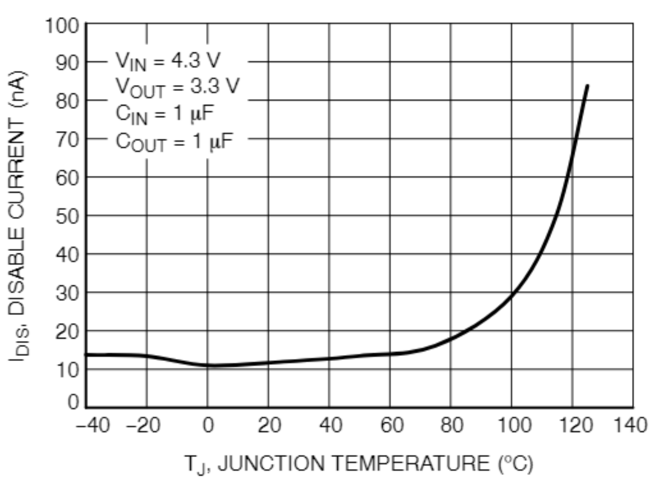


Figure 29. Disable Current vs. Temperature

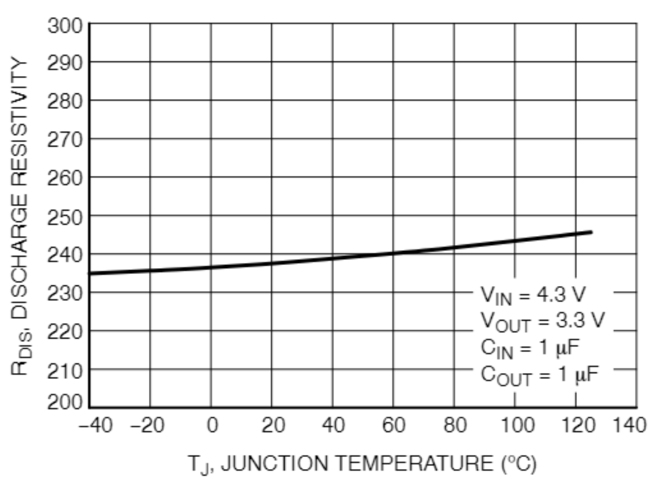
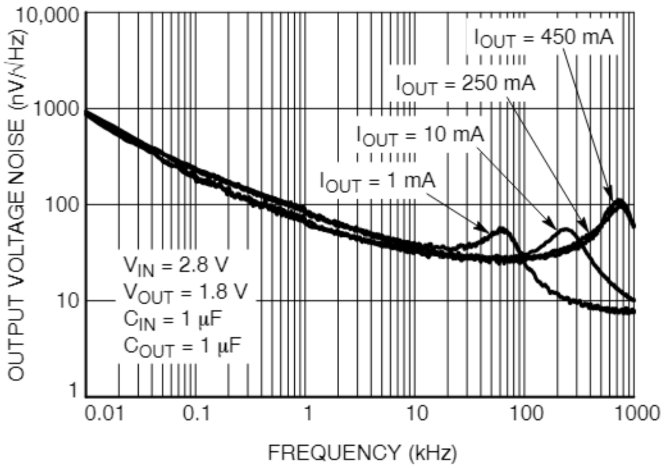


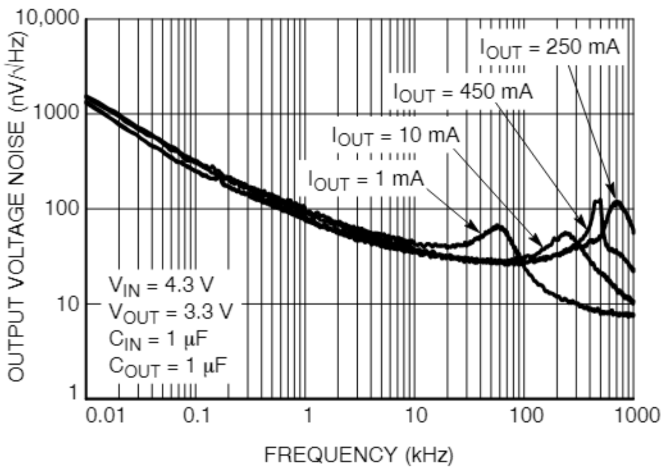
Figure 30. Discharge Resistivity vs. Temperature

TYPICAL CHARACTERISTICS



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	14.62	14.10
10 mA	11.12	10.48
250 mA	10.37	9.82
450 mA	10.22	9.62

Figure 31. Output Voltage Noise Spectral Density – V_{OUT} = 1.8 V



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	16.9	15.79
10 mA	12.64	11.13
250 mA	11.96	10.64
450 mA	11.50	10.40

Figure 32. Output Voltage Noise Spectral Density – V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS

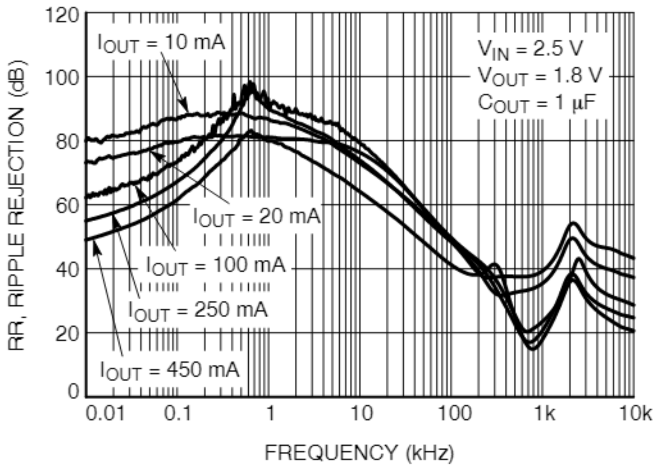


Figure 33. Power Supply Rejection Ratio, V_{OUT} = 1.8 V

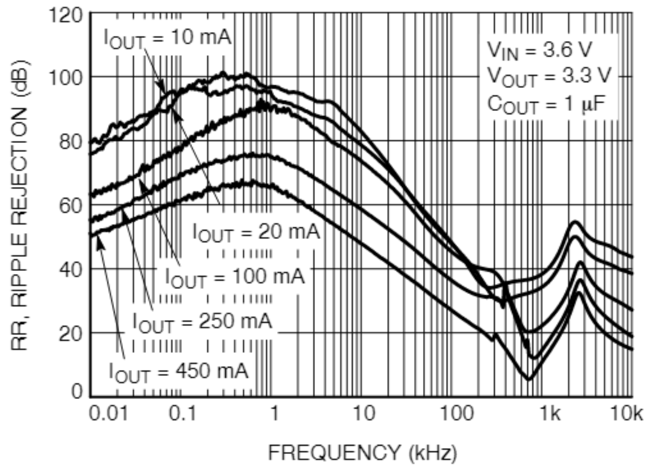


Figure 34. Power Supply Rejection Ratio, V_{OUT} = 3.3 V

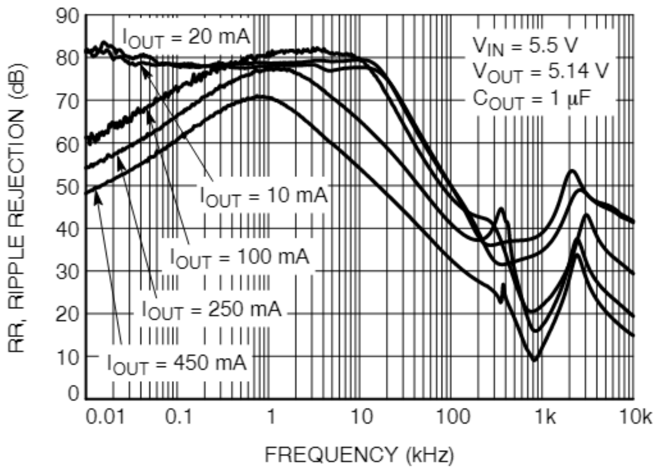


Figure 35. Power Supply Rejection Ratio, V_{OUT} = 5.14 V

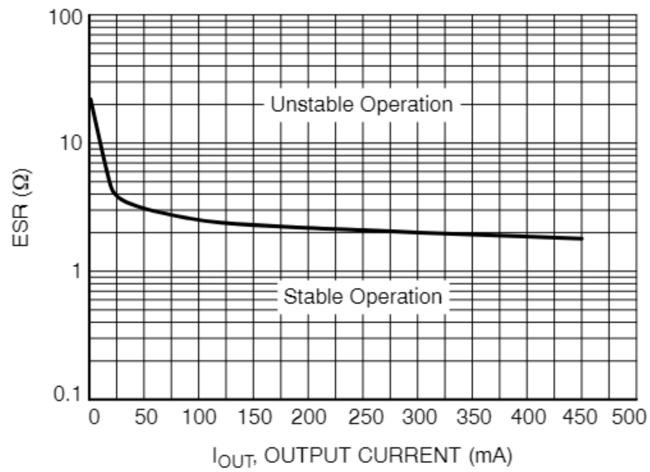


Figure 36. Stability vs. ESR

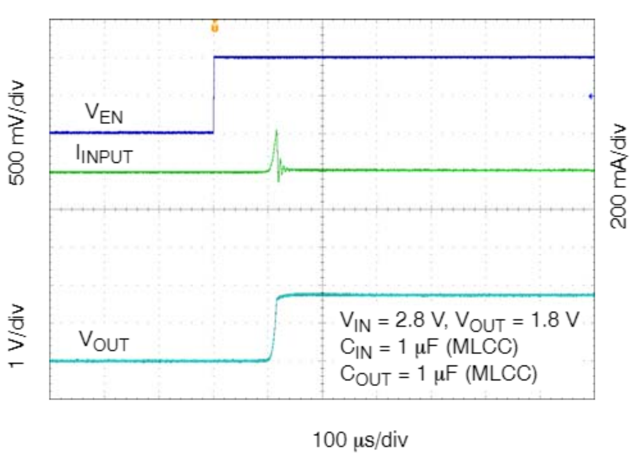


Figure 37. Enable Turn−on Response − C_{OUT} = 1 μF, I_{OUT} = 10 mA

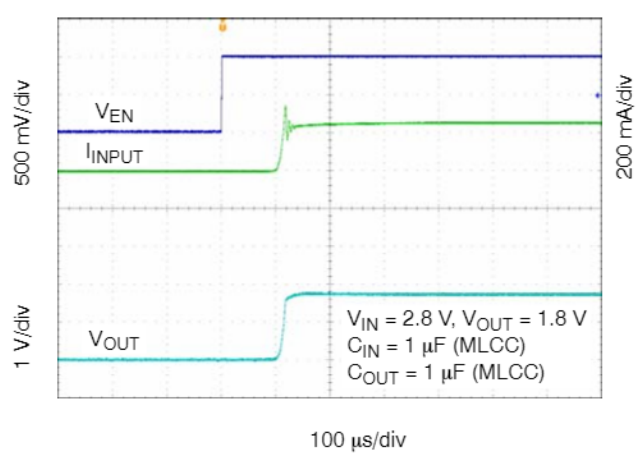


Figure 38. Enable Turn−on Response − C_{OUT} = 1 μF, I_{OUT} = 250 mA

TYPICAL CHARACTERISTICS

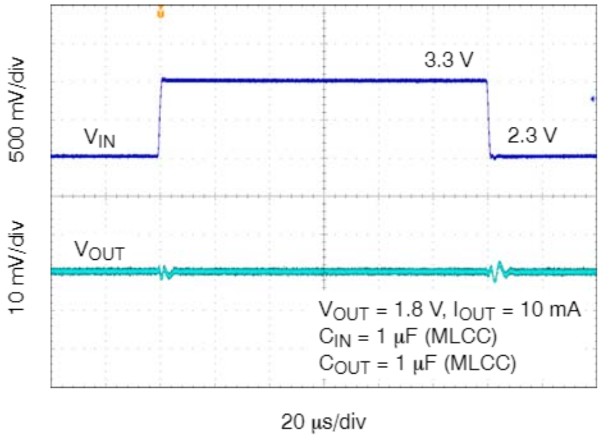


Figure 39. Line Transient Response – V_{OUT} = 1.8 V

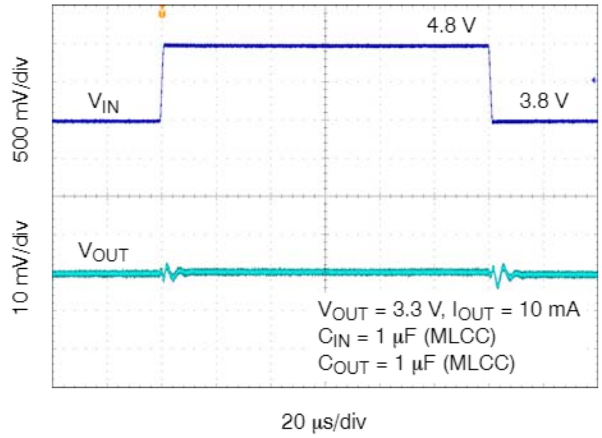


Figure 40. Line Transient Response – V_{OUT} = 3.3 V

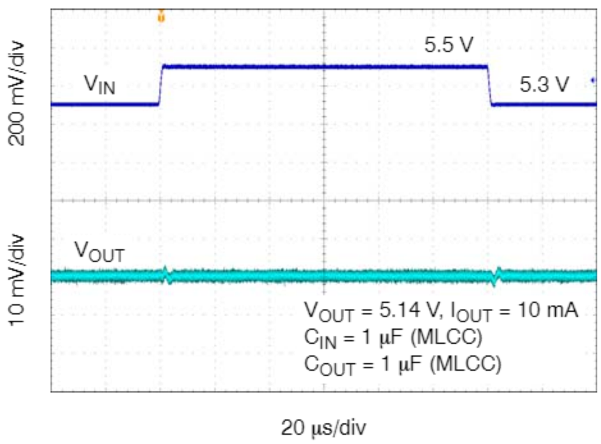


Figure 41. Line Transient Response – V_{OUT} = 5.14 V

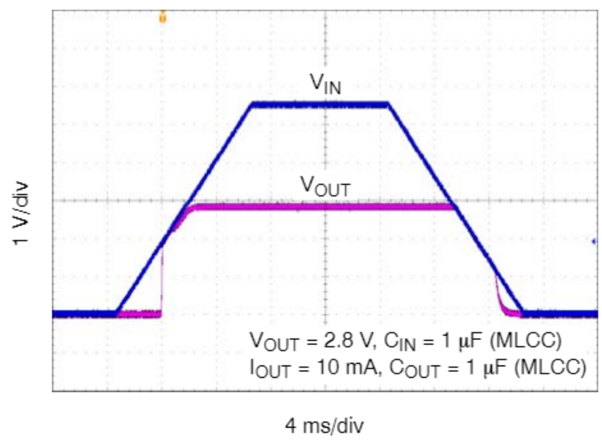


Figure 42. Turn–on/off – Slow Rising V_{IN}

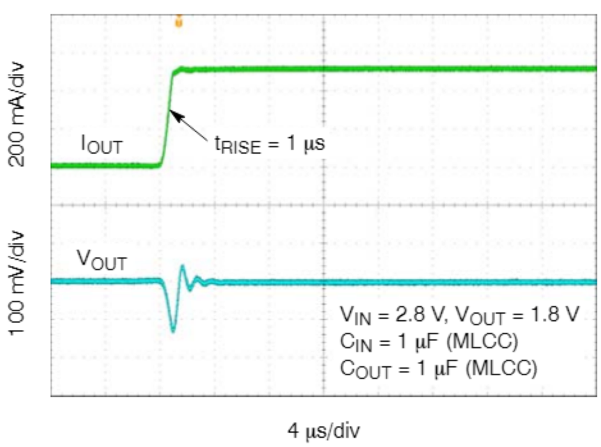


Figure 43. Load Transient Response – 1 mA to 450 mA – V_{OUT} = 1.8 V

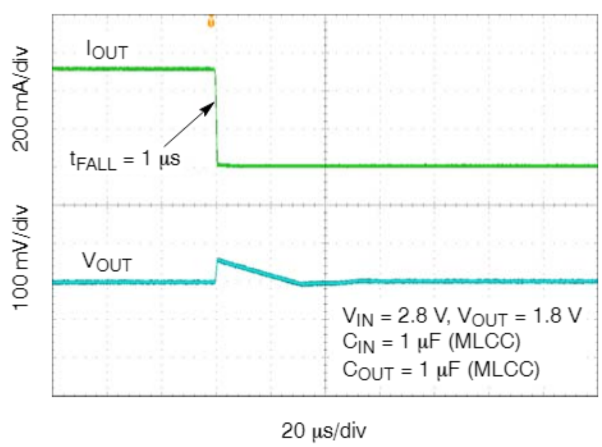


Figure 44. Load Transient Response – 450 mA to 1 mA – V_{OUT} = 1.8 V

TYPICAL CHARACTERISTICS

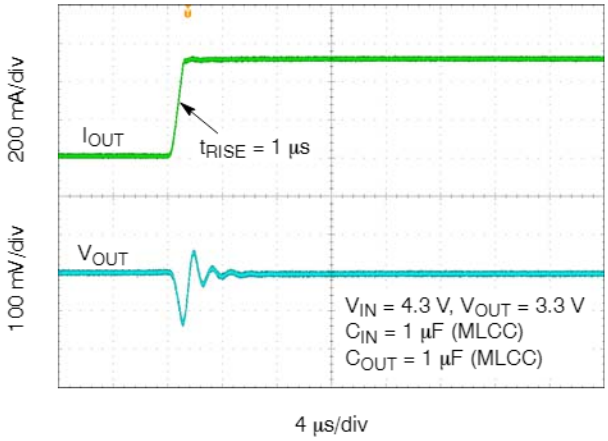


Figure 45. Load Transient Response – 1 mA to 450 mA – V_{OUT} = 3.3 V

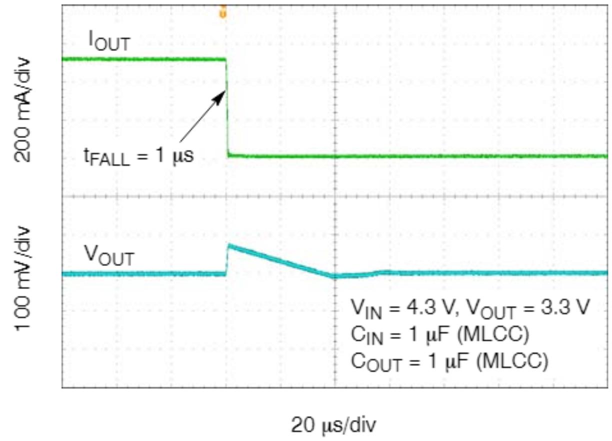


Figure 46. Load Transient Response – 450 mA to 1 mA – V_{OUT} = 3.3 V

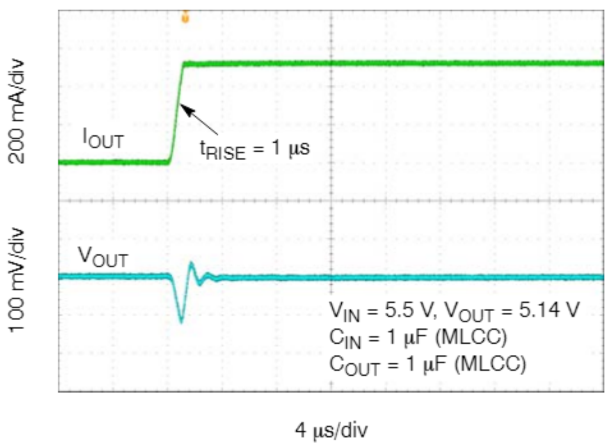


Figure 47. Load Transient Response – 1 mA to 450 mA – V_{OUT} = 5.14 V

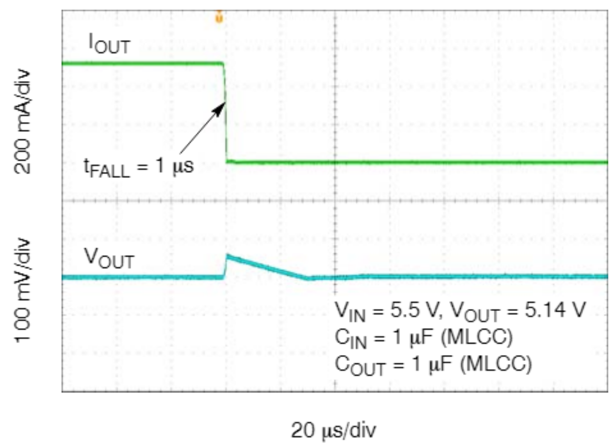


Figure 48. Load Transient Response – 450 mA to 1 mA – V_{OUT} = 5.14 V

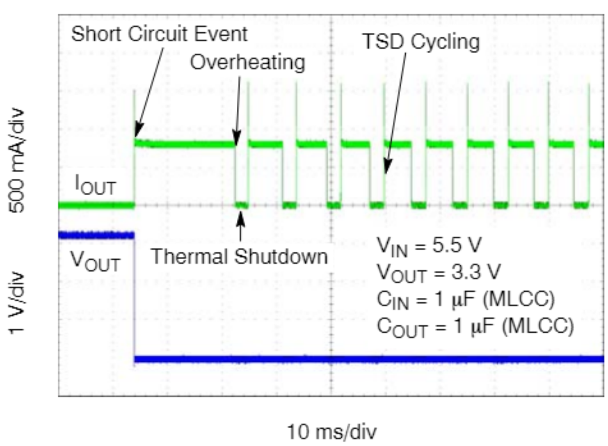


Figure 49. Short Circuit and Thermal Shutdown

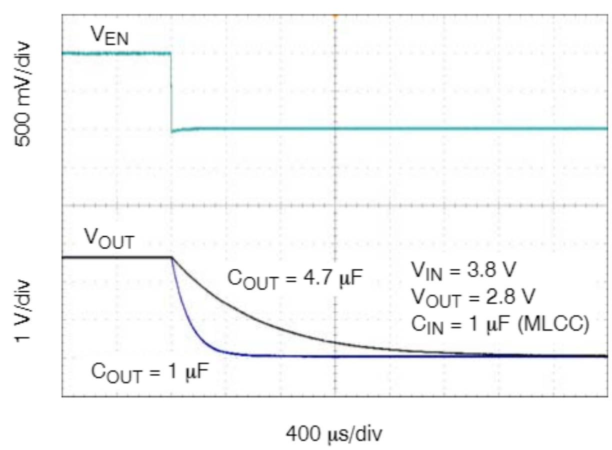


Figure 50. Enable Turn–off

APPLICATIONS INFORMATION

General

The NCP161 is an ultra−low noise 450 mA low dropout regulator designed to meet the requirements of RF applications and high performance analog circuits. The NCP161 device provides very high PSRR and excellent dynamic response. In connection with low quiescent current this device is well suitable for battery powered application such as cell phones, tablets and other. The NCP161 is fully protected in case of current overload, output short circuit and overheating.

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary for ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μF or greater to ensure the best dynamic performance. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Output Decoupling (C_{OUT})

The NCP161 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCP161 is designed to remain stable with minimum effective capacitance of 0.7 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias. Please refer Figure 51.

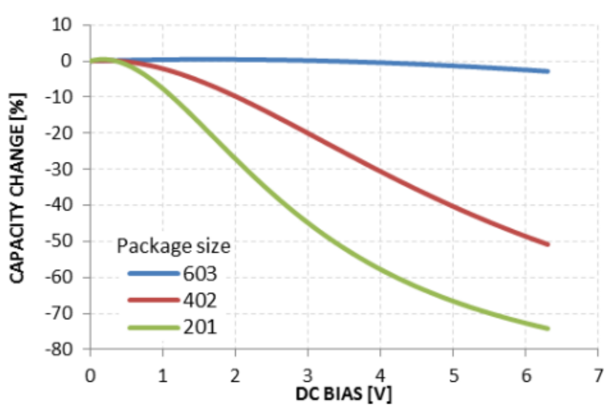


Figure 51. Capacity vs DC Bias Voltage

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 2 Ω. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature.

Enable Operation

The NCP161 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned−off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 280 Ω resistor. In the disable state the device consumes as low as typ. 10 nA from the V_{IN}.

If the EN pin voltage >1.2 V the device is guaranteed to be enabled. The NCP161 regulates the output voltage and the active discharge transistor is turned−off.

The EN pin has internal pull−down current source with typ. value of 200 nA which assures that the device is turned−off when the EN pin is not connected. In the case where the EN function isn't required the EN should be tied directly to IN.

Output Current Limit

Output Current is internally limited within the IC to a typical 700 mA. The NCP161 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 690 mA (typ). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCP161 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the NCP161 can handle is given by:

$$P_{D(MAX)} = \frac{\left[125°C - T_A\right]}{\theta_{JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCP161 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN} \cdot I_{GND} + I_{OUT}\left(V_{IN} - V_{OUT}\right) \quad \text{(eq. 2)}$$

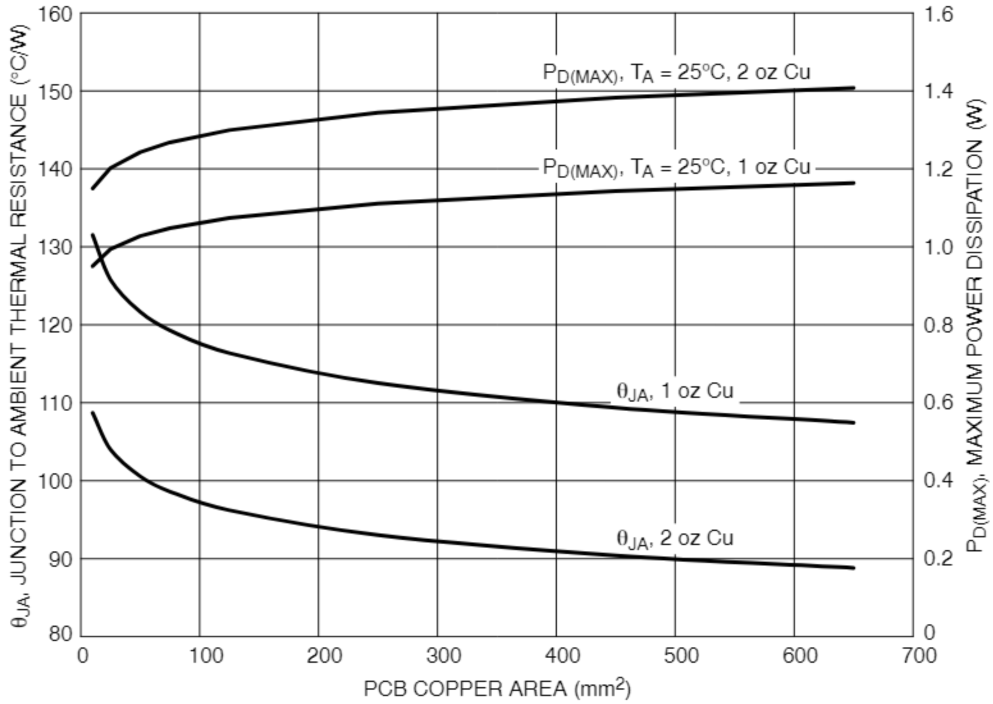


Figure 52. θ_{JA} and $P_{D\ (MAX)}$ vs. Copper Area (CSP4)

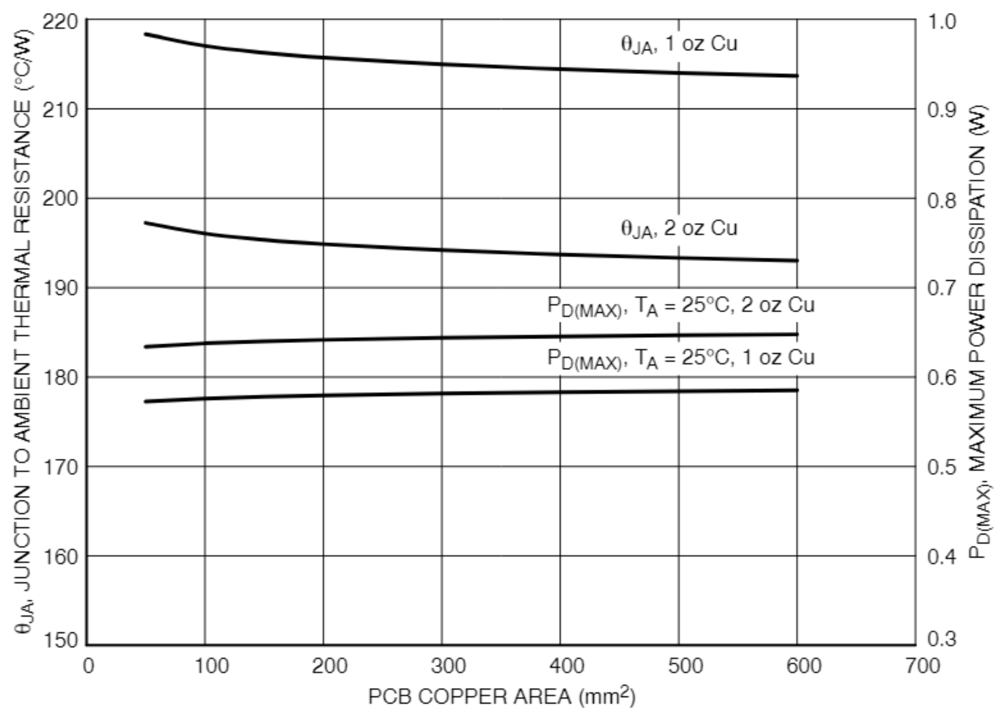


Figure 53. θ_{JA} and $P_{D\ (MAX)}$ vs. Copper Area (XDFN4)

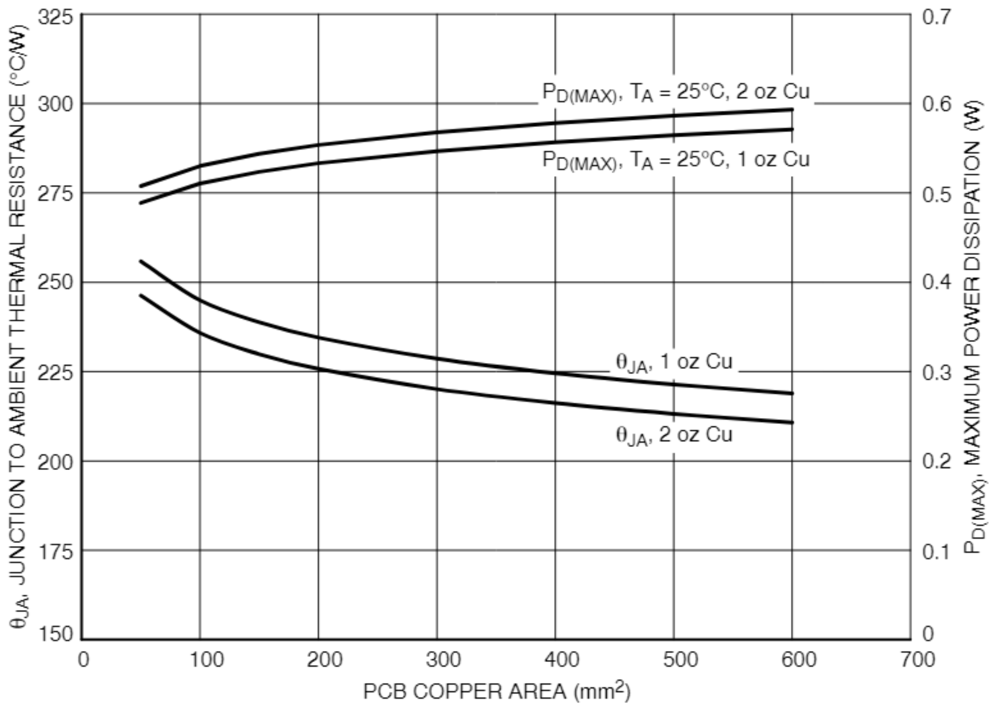


Figure 54. θ_{JA} and $P_{D\ (MAX)}$ vs. Copper Area (SOT23−5)

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The NCP161 features very high Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Turn−On Time

The turn−on time is defined as the time period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$, C_{OUT}, T_A.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 or 0201 capacitors with appropriate capacity. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad can be tied to the GND pin for improvement power dissipation and lower device temperature.

ORDERING INFORMATION

Device	Nominal Output Voltage	Description	Marking	Rotation	Package	Shipping
NCP161AFCS180T2G	1.8 V	450 mA, Active Discharge	A	180°	WLCSP4 CASE 567KA* (Pb-Free)	5000 / Tape & Reel
NCP161AFCS250T2G	2.5 V		D	180°		
NCP161AFCS270T2G	2.7 V		V	180°		
NCP161AFCS280T2G	2.8 V		E	180°		
NCP161AFCS285T2G	2.85 V		F	180°		
NCP161AFCS300T2G	3.0 V		J	180°		
NCP161AFCS320T2G	3.2 V		T	180°		
NCP161AFCS330T2G	3.3 V		K	180°		
NCP161AFCS350T2G	3.5 V		L	180°		
NCP161AFCS450T2G	4.5 V		P	180°		
NCP161AFCS500T2G	5.0 V		R	180°		
NCP161AFCS514T2G	5.14 V		Q	180°		
NCP161BFCS180T2G	1.8 V	450 mA, Non-Active Discharge	A	270°	WLCSP4 CASE 567KA* (Pb-Free)	5000 / Tape & Reel
NCP161BFCS250T2G	2.5 V		D	270°		
NCP161BFCS280T2G	2.8 V		E	270°		
NCP161BFCS285T2G	2.85 V		F	270°		
NCP161BFCS300T2G	3.0 V		J	270°		
NCP161BFCS330T2G	3.3 V		K	270°		
NCP161BFCS350T2G	3.5 V		L	270°		
NCP161BFCS450T2G	4.5 V		P	270°		
NCP161BFCS500T2G	5.0 V		R	270°		
NCP161BFCS514T2G	5.14 V		Q	270°		
NCP161AFCT180T2G	1.8 V	450 mA, Active Discharge	A	180°	WLCSP4 CASE 567JZ (Pb-Free)	5000 / Tape & Reel
NCP161AFCT185T2G	1.85 V		V	180°		
NCP161AFCT250T2G	2.5 V		D	180°		
NCP161AFCT280T2G	2.8 V		E	180°		
NCP161AFCT285T2G	2.85 V		F	180°		
NCP161AFCT290T2G	2.9 V		T	180°		
NCP161AFCT300T2G	3.0 V		J	180°		
NCP161AFCT310T2G	3.1 V		6	180°		
NCP161AFCT330T2G	3.3 V		K	180°		
NCP161AFCT350T2G	3.5 V		L	180°		
NCP161AFCT450T2G	4.5 V		P	180°		
NCP161AFCT500T2G	5.0 V		R	180°		
NCP161AFCT514T2G	5.14 V		Q	180°		
NCP161AFCTC280T2G	2.8 V	450 mA, Active Discharge, Backside Coating	E	180°		
NCP161AFCTC350T2G	3.5 V		L	180°		
NCP161BFCT180T2G	1.8 V	450 mA, Non-Active Discharge	A	270°	WLCSP4 CASE 567JZ (Pb-Free)	5000 / Tape & Reel
NCP161BFCT185T2G	1.85 V		V	270°		
NCP161BFCT250T2G	2.5 V		D	270°		
NCP161BFCT280T2G	2.8 V		E	270°		
NCP161BFCT285T2G	2.85 V		F	270°		
NCP161BFCT300T2G	3.0 V		J	270°		
NCP161BFCT330T2G	3.3 V		K	270°		
NCP161BFCT350T2G	3.5 V		L	270°		
NCP161BFCT450T2G	4.5 V		P	270°		
NCP161BFCT500T2G	5.0 V		R	270°		
NCP161BFCT514T2G	5.14 V		Q	270°		

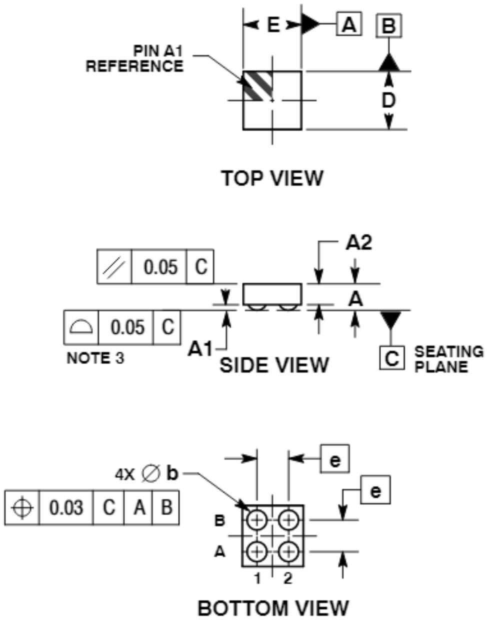
*UBM = 180 μm (±5 μm)

ORDERING INFORMATION

Device	Nominal Output Voltage	Description	Marking	Package	Shipping
NCP161AMX180TBG	1.8 V	450 mA, Active Discharge	DN	XDFN4 (Pb-Free)	3000 / Tape & Reel
NCP161AMX185TBG	1.85 V		EY		
NCP161AMX250TBG	2.5 V		DP		
NCP161AMX280TBG	2.8 V		DQ		
NCP161AMX285TBG	2.85 V		DR		
NCP161AMX300TBG	3.0 V		DT		
NCP161AMX320TBG	3.2 V		DZ		
NCP161AMX330TBG	3.3 V		DD		
NCP161AMX350TBG	3.5 V		DU		
NCP161AMX450TBG	4.5 V		DV		
NCP161AMX500TBG	5.0 V		DX		
NCP161AMX514TBG	5.14 V		DE		
NCP161BMX180TBG	1.8 V	450 mA, Non-Active Discharge	EN	XDFN4 (Pb-Free)	3000 / Tape & Reel
NCP161BMX250TBG	2.5 V		EP		
NCP161BMX280TBG	2.8 V		EQ		
NCP161BMX285TBG	2.85 V		ER		
NCP161BMX300TBG	3.0 V		ET		
NCP161BMX330TBG	3.3 V		ED		
NCP161BMX350TBG	3.5 V		EU		
NCP161BMX450TBG	4.5 V		EV		
NCP161BMX500TBG	5.0 V		EW		
NCP161BMX514TBG	5.14 V		EE		
NCP161ASN180T1G	1.8 V	450 mA, Active Discharge	JAF	SOT23−5L (Pb-Free)	3000 / Tape & Reel
NCP161ASN250T1G	2.5 V		JAA		
NCP161ASN280T1G	2.8 V		JAC		
NCP161ASN300T1G	3.0 V		JAD		
NCP161ASN330T1G	3.3 V		JAG		
NCP161ASN350T1G	3.5 V		JAH		
NCP161ASN500T1G	5.0 V		JAE		

PACKAGE DIMENSIONS

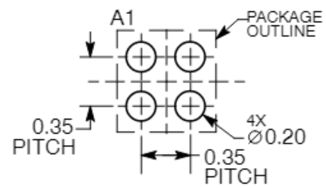
WLCSP4, 0.64x0.64
CASE 567JZ
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS MIN	NOM	MAX
A	---	---	0.33
A1	0.04	0.06	0.08
A2	0.23 REF		
b	0.195	0.210	0.225
D	0.610	0.640	0.670
E	0.610	0.640	0.670
e	0.35 BSC		

RECOMMENDED SOLDERING FOOTPRINT*

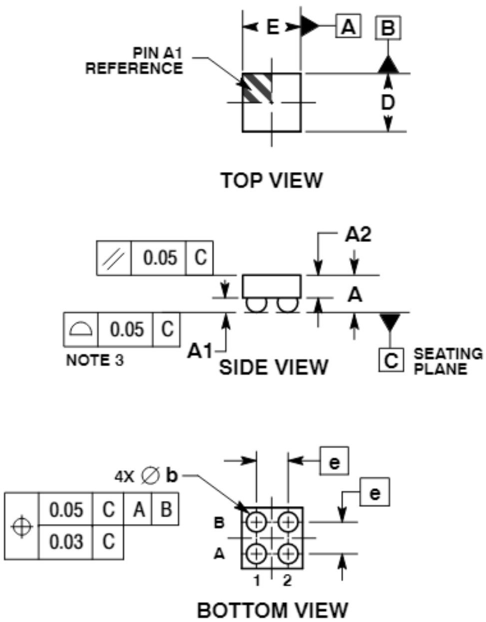


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

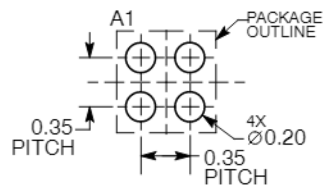
WLCSP4, 0.64x0.64
CASE 567KA
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**
A	0.35	0.40	0.45
A1	0.14	0.16	0.18
A2	0.25 REF		
b	0.185	0.200	0.215
D	0.610	0.640	0.670
E	0.610	0.640	0.670
e	0.35 BSC		

RECOMMENDED SOLDERING FOOTPRINT*

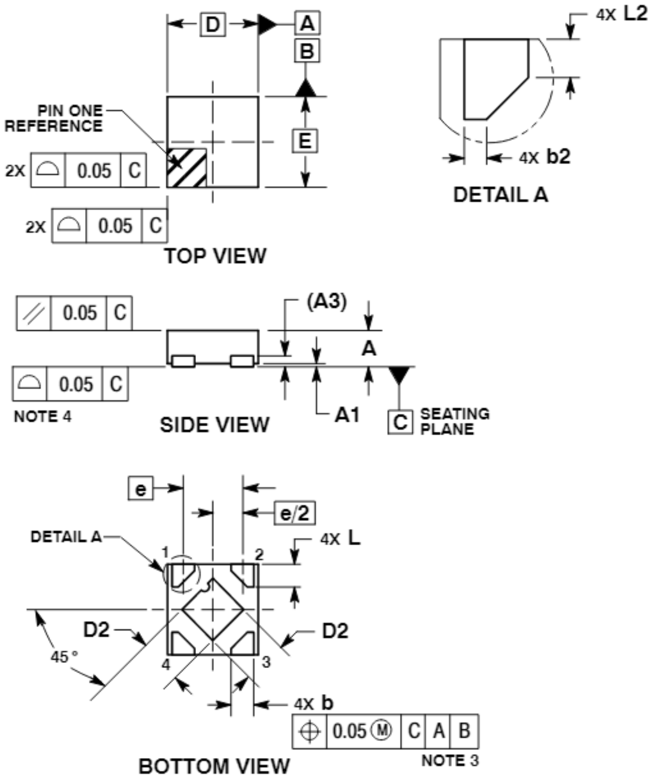


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

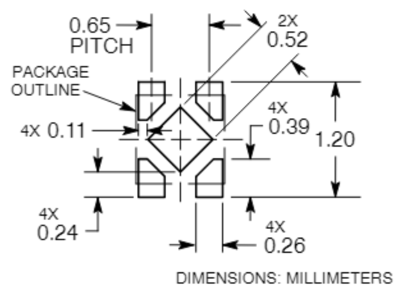
XDFN4 1.0x1.0, 0.65P
CASE 711AJ
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.33	0.43
A1	0.00	0.05
A3	0.10 REF	
b	0.15	0.25
b2	0.02	0.12
D	1.00 BSC	
D2	0.43	0.53
E	1.00 BSC	
e	0.65 BSC	
L	0.20	0.30
L2	0.07	0.17

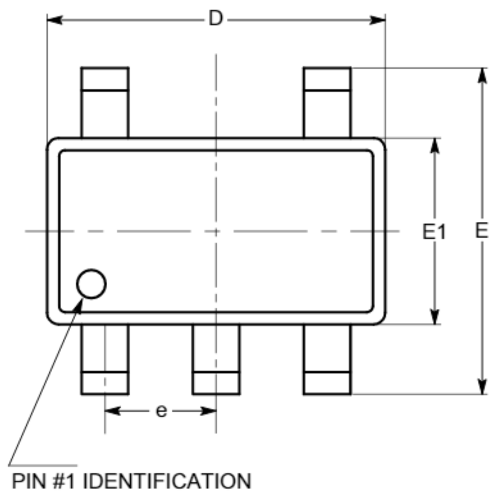
RECOMMENDED MOUNTING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

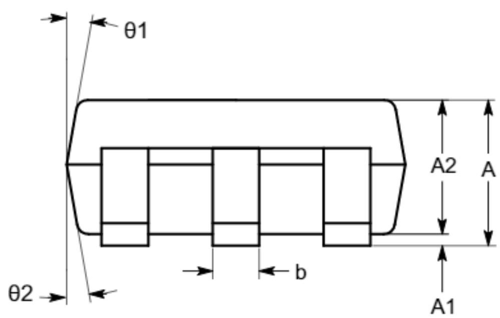
PACKAGE DIMENSIONS

SOT−23, 5 Lead
CASE 527AH
ISSUE O

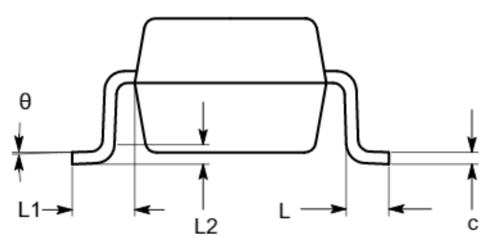


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.90		1.45
A1	0.00		0.15
A2	0.90	1.15	1.30
b	0.30		0.50
c	0.08		0.22
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
e		0.95 BSC	
L	0.30	0.45	0.60
L1		0.60 REF	
L2		0.25 REF	
θ	0°	4°	8°
θ1	5°	10°	15°
θ2	5°	10°	15°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions in millimeters. Angles in degrees.
(2) Complies with JEDEC standard MO-178.

PUBLICATION ORDERING INFORMATION

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