

## 10.5V Fast Startup with F0 Detect and Tracking LRA Haptic Driver

### FEATURES

- 1MHz I<sup>2</sup>C Bus Control(Address: 0x5A/0x5B)
- LRA Resonant Frequency Detect and Tracking Option
- LRA Fault Diagnostics based on Resistance
- Drive Compensation Over Battery Discharge
- Integrated 8-KByte Internal Waveform Memory
- Up to 4-KByte Configurable FIFO Interface
- Flexible Playback Modes:  
Real Time Playback, Memory Playback,  
Hardware Trigger Playback and CONT Playback
- 1.2ms Fast Start Up Time
- Support  $\geq 8\Omega$  LRA
- Up to 3 Hardware Pins Trigger Input
- Dedicated Interrupt Output Pin
- High Voltage H-Bridge Driver
- Integrated Boost Output Voltage up to 10.5V
- Support Automatically Switch to Standby Mode
- Standby Current: 8 $\mu$ A
- Shutdown Current: 0.2 $\mu$ A
- 3V to 5.5V Supply Voltage Range
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection
- FCQFN 3mm x 2mm x 0.55mm -20L Package

### APPLICATIONS

- Mobile phones
- Tablets
- Wearable Devices

### DESCRIPTION

The device is the high voltage H-bridge, single chip LRA haptic driver, with LRA resonant frequency detect and tracking, with an integrated boost converter and integrated waveform memory, supporting real time playback and hardware pin trigger playback. Maximum drive voltage is up to 10.5V and a typical startup time of 1.2ms makes the device an ideal haptic driver for fast responses.

The device supports software controlled LRA resonant frequency(F0) detect, it can detect the actual F0 after LRA delivered to customer or the actual F0 after LRA mounted in the mobile.

The device supports LRA resonant frequency tracking based on LRA BEMF. It supports automatically tracks and generates the LRA resonant frequency.

The device supports LRA fault diagnostic based on resistance measurement.

The device supports real time playback for long waveform play. Software trigger and hardware trigger are supported for different applications.

The device integrates a high-efficiency boost converter as the H-Bridge driver supply rail. The output voltage, maximum current limit and maximum boost current are configurable.

The device features configurable automatically switch to standby mode. This can less quiescent power consumption. Dedicated interrupt output pin can detect real time FIFO status and the error status of the chip.

The device offers short circuit protection, over-temperature protection, under-voltage protection to protect the device.

The device features general settings are communicated via an I<sup>2</sup>C -bus interface and its I<sup>2</sup>C address is configurable.

The device is available in a FCQFN 3mm x 2mm x 0.55mm -20L package.

*All trademarks are the property of their respective owners.*

## PIN CONFIGURATION AND TOP MARK

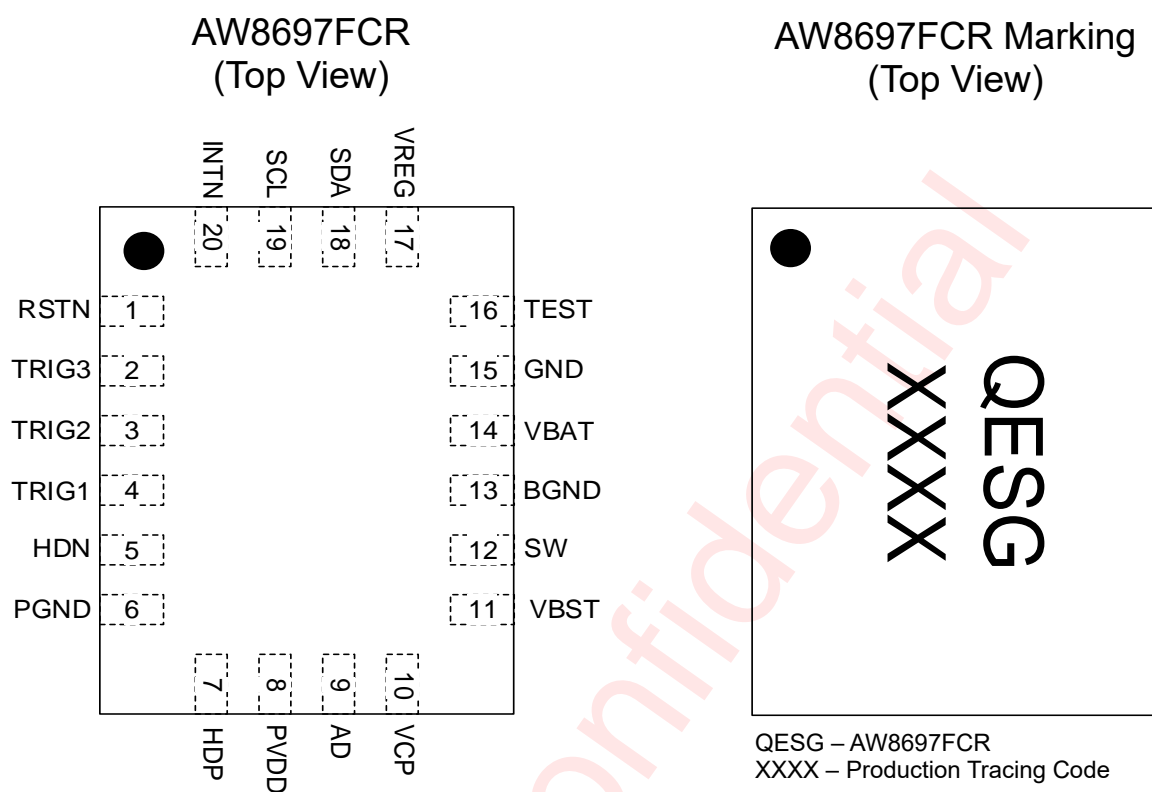


Figure 1 Pin Configuration and Top Mark

## PIN DEFINITION

NAME	PIN NUMBER	DESCRIPTION
RSTN	1	Active low hardware reset. High: standby/active mode Low: power-down mode
TRIG3	2	Hardware trigger 3
TRIG2	3	Hardware trigger 2
TRIG1	4	Hardware trigger 1
HDN	5	Negative haptic driver differential output
PGND	6	H-bridge driver GND
HDP	7	Positive haptic driver differential output
PVDD	8	High voltage driver power rail
AD	9	I <sup>2</sup> C bus address selection
VCP	10	Internal charge pump voltage
VBST	11	Boost output voltage
SW	12	Internal boost switch pin
BGND	13	Boost GND
VBAT	14	Chip power supply
GND	15	Ground
TEST	16	Test output pin, must leave it unconnected
VREG	17	Digital power supply
SDA	18	I <sup>2</sup> C bus data input/output
SCL	19	I <sup>2</sup> C bus clock input
INTN	20	Interrupt open drain output, low active

## FUNCTIONAL BLOCK DIAGRAM

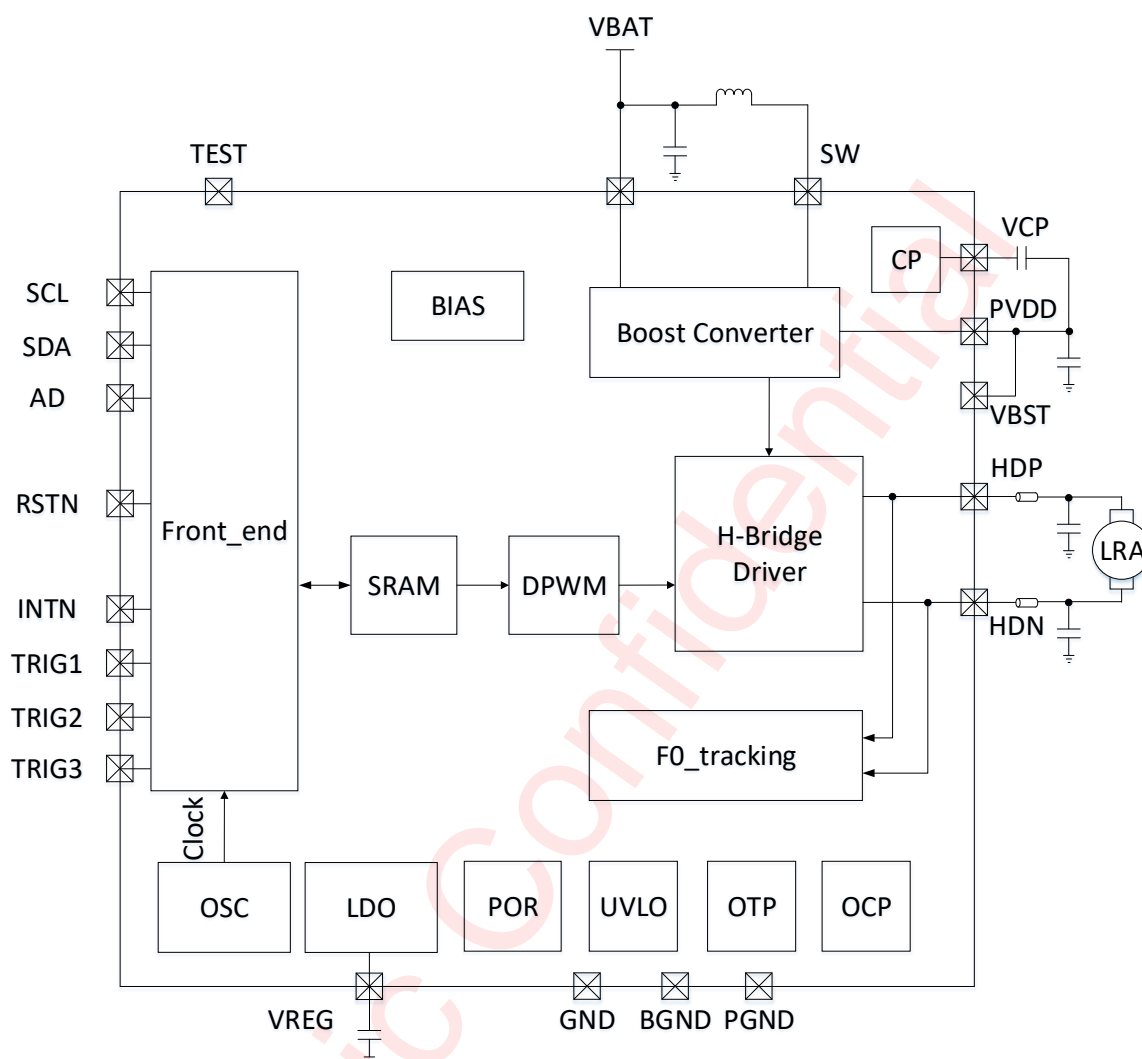


Figure 2 Functional Block Diagram

## TYPICAL APPLICATION CIRCUITS

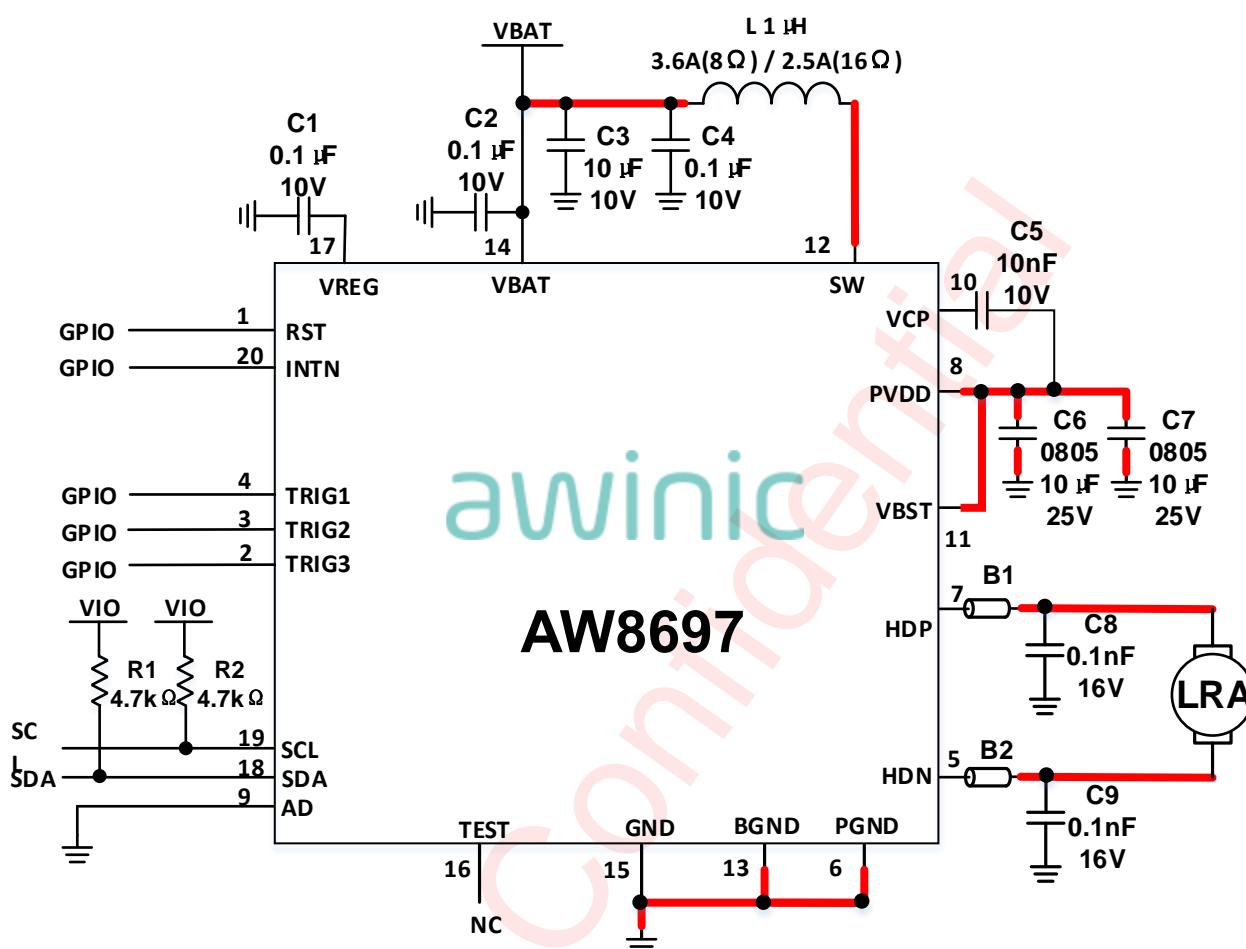


Figure 3 Typical Application Circuit of AW8697

All trademarks are the property of their respective owners.

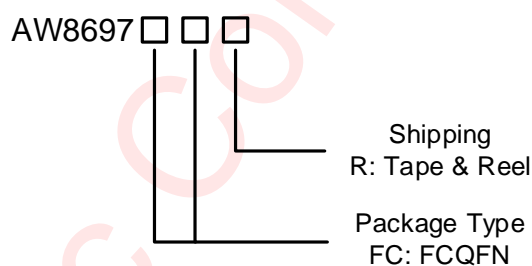
**Notice for Typical Application Circuits:**

1: Please place C1, C2, C3, C4, C5, C6, C7 as close to the chip as possible, and C6 and C7 close to PIN 11 and the capacitors should be placed in the same layer with the device.

2: For the sake of driving capability, the power lines (especially the one to Pin 12), output lines, and the connection lines of L1, and SW should be short and wide as possible. The power path marked in red as shown in the figures above. Please traces according to 1.5A power line alignment rules, for VBAT to SW through L1. and the other red path traces according to 1.5A power line alignment rules.

**ORDERING INFORMATION**

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environment Information	Delivery Form
AW8697FCR	-40°C ~ 85°C	FCQFN 3mmX2mm-20L	QESG	MSL1	ROHS+HF	6000 units/ Tape and Reel



**ABSOLUTE MAXIMUM RATINGS**(NOTE 1)

PARAMETER	RANGE
Battery Supply Voltage VBAT	-0.3V to 6.0V
Digital power supply VREG	-0.3V to 2.0V
Internal charge pump voltage VCP	-0.3V to 17V
Boost output voltage VBST PVDD	-0.3V to 12V
Internal boost switch pin SW	-0.3V to 15V
HDP, HDN	-0.3V to PVDD+0.3V
Minimum load resistance R <sub>L</sub>	5Ω
Package Thermal Resistance θ <sub>JA</sub>	60°C/W
Ambient Temperature Range	-40°C to 85°C
Maximum Junction Temperature T <sub>JMAX</sub>	165°C
Storage Temperature Range T <sub>STG</sub>	-65°C to 150°C
Lead Temperature(Soldering 10 Seconds)	260°C
<b>ESD Rating</b> (NOTE 2 3 4)	
HBM(Human Body Model)	±2000V
CDM(Charge Device Model)	±2000V
MM(Machine Model)	±200V
<b>Latch-Up</b>	
Test Condition: JESD78E	+IT: 800mA -IT: -800mA

NOTE 1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE 2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.  
Test method: ESDA/JEDEC JS-001-2017.

NOTE 3: Charge Device Model test method: ESDA/JEDEC JS-002-2014.

NOTE 4: Machine Model test method: JESD22-A115C.

## ELECTRICAL CHARACTERISTICS

## CHARACTERISTICS

Test condition: TA=25°C, VBAT=3.6V, PVDD=8.5V, RL=8Ω+100μH(unless otherwise noted)

Symbol	Description	Test Conditions	MIN	TYP	MAX	Units
VBAT	Battery supply voltage	On pin VBAT	3		5.5	V
V <sub>VREG</sub>	Voltage at VREG pin			1.8		V
V <sub>IL</sub>	Logic input low level	RSTN/TRIG1/TRIG2/ TRIG3/AD/ SCLK			0.5	V
V <sub>IH</sub>	Logic input high level	RSTN/TRIG1/TRIG2/ TRIG3/AD/ SCLK	1.3			V
V <sub>OL</sub>	Logic output low level	INTN/TEST/SDA I <sub>OUT</sub> =4mA			0.4	V
V <sub>OH</sub>	Logic output high level	TEST I <sub>OUT</sub> =4mA	1.3			V
V <sub>OS</sub>	Output offset voltage	I2C signal input 0	-30	0	30	mV
I <sub>SD</sub>	Shutdown current	VBAT=4.2V, RSTN =0V		0.2	1	μA
I <sub>STBY</sub>	Standby current	VBAT=3.6V, AD=0V TRIG1=TRIG2=TRIG3=0V RSTN=SCL=SDA=1.8V		8		μA
I <sub>Q</sub>	Quiescent current	VBAT=3.6V, PVDD=8.5V		10.2		mA
UVP	Under-voltage protection voltage			2.7		V
	Under-voltage protection hysteresis voltage			100		mV
T <sub>SD</sub>	Over temperature protection threshold			160		°C
T <sub>SDR</sub>	Over temperature protection recovery threshold			130		°C
T <sub>START</sub>	Waveform startup time	From trigger to output signal		1.2		ms
<b>BOOST</b>						
PVDD	Boost output voltage	VBAT=3V to 5.5V		8.5		V
OVP	Over-voltage threshold			1.1* V <sub>PVDD</sub>		
F <sub>BST</sub>	Operating Frequency			1.6		MHz
D <sub>MAX</sub>	The maximum duty cycle			90%		
I <sub>L_PEAK</sub>	Inductor peak current limit				4	A
T <sub>ST</sub>	Soft-start time	No load, C <sub>OUT</sub> =22μF		0.3		ms



HDRIVER						
$R_{dson}$	Drain-Source on-state resistance	Include NMOS and PMOS		350		mΩ
$R_{ocp}$	Load impedance threshold for over current protection	VBAT=3.6V, PVDD=8.5V		2		Ω
FPWM	PWM Output Frequency	VBAT=4.2V, PWMCLK_MODE = 0		48		kHz
		VBAT=4.2V, PWMCLK_MODE = 2		24		kHz
		VBAT=4.2V, PWMCLK_MODE = 3		12		kHz
$F_{CALI\_ACC\_LRA}$	LRA Consistency Calibration Accuracy		-2	F0	2	Hz
$V_{peak}$	Output Voltage	RL=16Ω+100μH, VBAT=4.2V, PVDD=8.0V		7.7		V
	Output Voltage	RL=8Ω+100μH, VBAT=4.2V, PVDD=8.0V		7.5		V

I<sup>2</sup>C INTERFACE TIMING

No.	Symbol	Parameter Name	Fast mode			Fast mode Plus			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
1	f <sub>SCL</sub>	SCL Clock frequency			400			1000	kHz
2	t <sub>LOW</sub>	SCL Low level Duration	1.3			0.5			μs
3	t <sub>HIGH</sub>	SCL High level Duration	0.6			0.26			μs
4	t <sub>RISE</sub>	SCL, SDA rise time			0.3			0.12	μs
5	t <sub>FALL</sub>	SCL, SDA fall time			0.3			0.12	μs
6	t <sub>SU:STA</sub>	Setup time SCL to START state	0.6			0.26			μs
7	t <sub>HD:STA</sub>	(repeat-start) start condition hold time	0.6			0.26			μs
8	t <sub>SU:STO</sub>	Stop condition setup time	0.6			0.26			μs
9	t <sub>BUF</sub>	Time between start and stop condition	1.3			0.5			μs
10	t <sub>SU:DAT</sub>	SDA setup time	0.1			0.05			μs
11	t <sub>HD:DAT</sub>	SDA hold time	10			10			ns

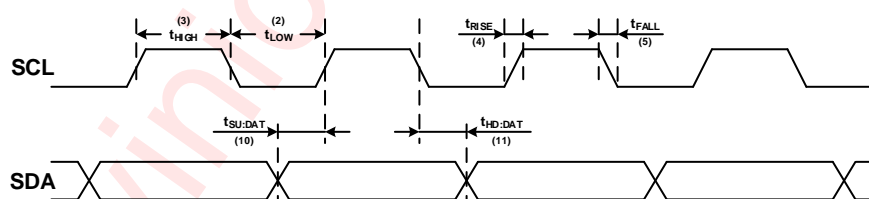


Figure 4 SCL and SDA Timing Relationships in The Data Transmission Process

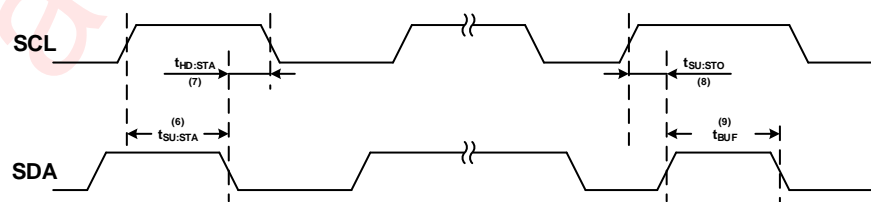


Figure 5 The Timing Relationship Between START And STOP State

## MEASUREMENT SETUP

AW8697 features switching digital output, as shown in Figure 6. Need to connect a low pass filter to HDP/HDN output respectively to filter out switch modulation frequency, then measure the differential output of filter to obtain analog output signal.

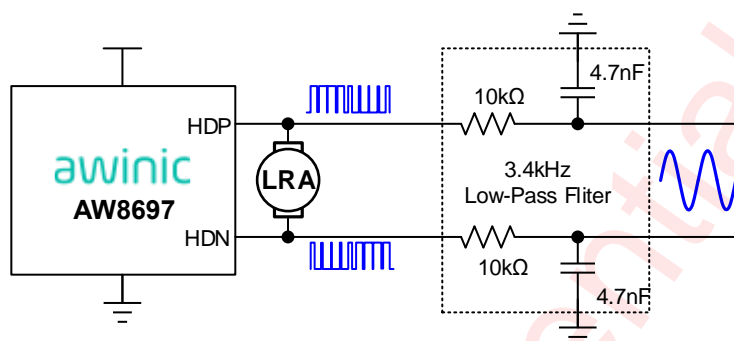


Figure 6 AW8697 Test Setup

## TYPICAL CHARACTERISTICS

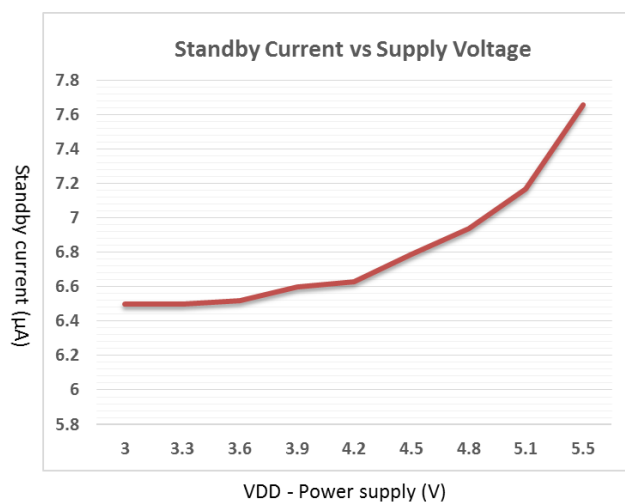


Figure 7 Standby Current vs Supply Voltage

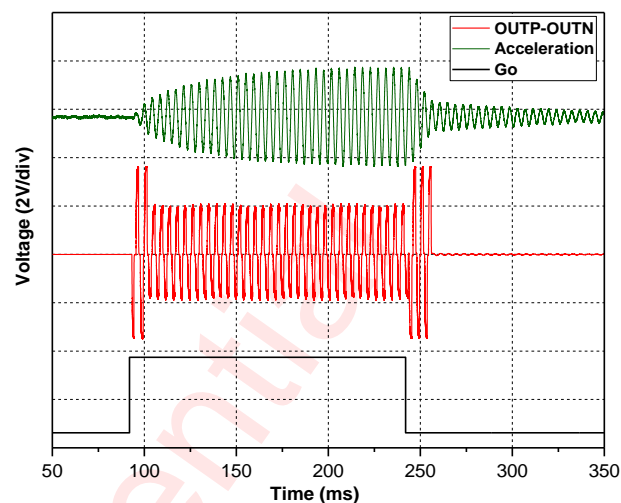


Figure 8 Long Vibration with Automatic Braking

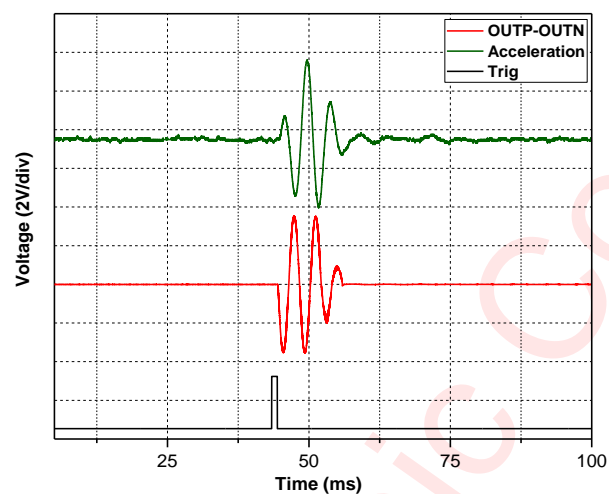


Figure 9 Click(Open-Loop) with External Trig

## DETAILED FUNCTIONAL DESCRIPTION

### POWER ON RESET

The device provides a power-on reset feature that is controlled by VREG OK. The reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers. When the VBAT power on, the VREG voltage raises and produce the OK indication, the reset is over.

The interrupt bit SYSINT.UVLI will be set to 1 when power-on reset operation occurs, which will be cleared by a read operation of SYSINT register. Usually the SYSINT.UVLI bit can be used to check whether an unexpected power-on event has taken place.

### OPERATION MODE

The device supports three operation modes.

Table 1 Operating Mode

Mode	Condition	Description
<b>Power-Down</b>	$V_{DD} = 0V$ or $RSTN = 0V$	Power supply is not ready or RSTN is tie to low. Whole chip shutdown including I <sup>2</sup> C interface.
<b>Standby</b>	$V_{DD} > 2.7V$ and $RSTN = 1$ and $STANDBY = 1$	Power supply is ready and RSTN is tie to high. Most parts of the device are power down for low power consumption except I <sup>2</sup> C interface and LDO.
<b>Active</b>	$STANDBY = 0$	Driver is ready for operating

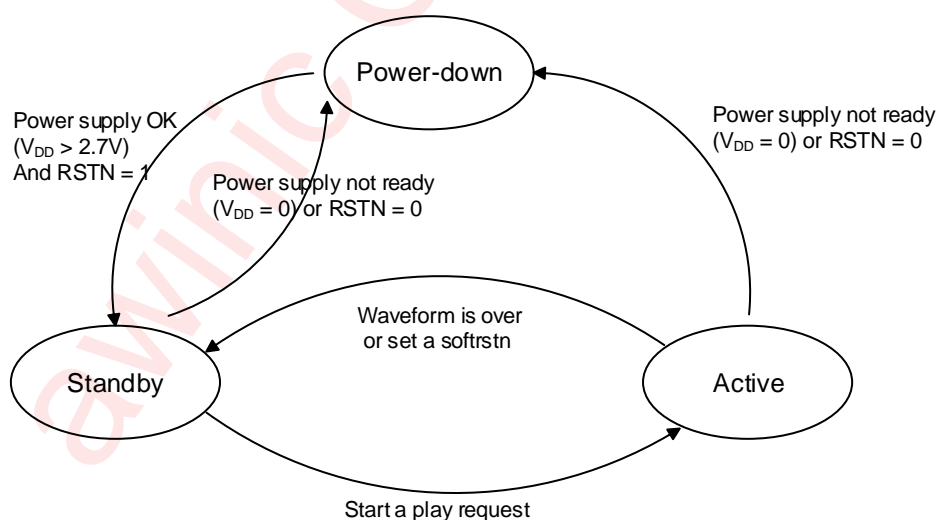


Figure 10 Device Operating Modes Transition

### POWER-DOWN MODE

The device switches to power-down mode when the supply voltage is not ready or RSTN pin is set to low. In this mode, all circuits inside this device will be shut down. I<sup>2</sup>C interface isn't accessible in this mode, and all of the internal configurable registers are cleared.

The device will jump out of the power-down mode automatically when the supply voltages are OK and RSTN pin is set to high.

## STANDBY MODE

The device switches standby mode when the power supply voltages are OK and RSTN pin set to high. In this mode I<sup>2</sup>C interface is accessible, other modules except LDO module are still powered down. Customer can set device to this mode when the device is no needed to work by setting STANDBY to high. Also in this mode, customer can initialize waveform library in SRAM. Device can be switched to this mode after haptic waveform playback finished.

## ACTIVE MODE

The device is fully operational in this mode. Boost and H-bridge driver circuits will start to work. Customer can set STANDBY = 0 to make device in this mode.

## POWER ON AND PLAYBACK SEQUENCE

This device power on sequence is illustrated in the following figure:

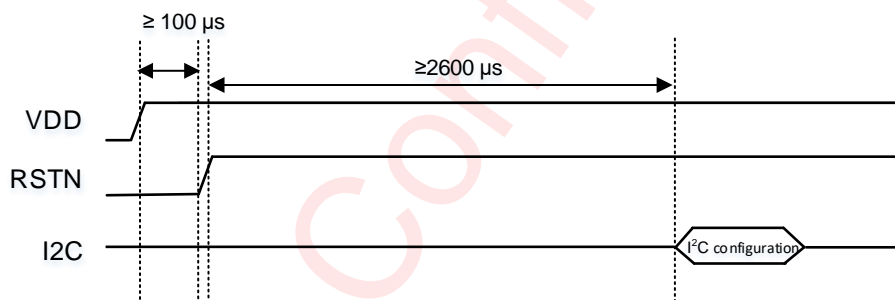


Figure 11 Power On Sequence

And the detail description of playback sequence for each step is listed in the following table:

Table 2 Detail Description of Playback Sequence

Step	description	Mode
1	Wait for VDD supply power on and RSTN to 1	Power-Down
2.1	Waveform library initialization in SRAM	Standby
2.2	Trig mode waveform configuring	Standby
2.3	RAM mode waveform configuring	Standby
2.4	Set playback mode or apply trig pulse signal to trig pins	Standby or Active
3	Set GO to 1 or additionally write data to RTP_DATA to trig playback	Active

## POWER DOWN SEQUENCE

This device power down sequence is illustrated in the following figure:

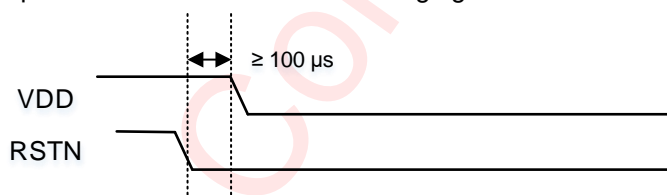


Figure 12 Power Down Sequence

## SOFTWARE RESET

Writing 0xAA to register CHIPID(0x00) via I<sup>2</sup>C interface will reset the device internal circuits and all configuration registers. After the software reset command is input through I<sup>2</sup>C, it needs to wait at least **1ms** before any other I<sup>2</sup>C command can be accepted.

## BATTERY VOLTAGE DETECT

Software can send command to detect the battery voltage. The register VBATDET[7:0] report this information.

## CONSTANT VIBRATION STRENGTH

The device features power-supply feedback. If the supply voltage discharge over time, the vibration strength remains the same as long as enough supply voltage is available to sustain the required output voltage. It is especially useful for ring application.

## LRA CONSISTENCY CALIBRATION

Different motor batches, assembly conditions and other factors can result in  $f_0$  deviation of LRA. When the drive waveform does not match the LRA monomer, the vibration may be inconsistent and the braking effect becomes worse, especially for short vibration waveforms. So it's necessary to perform consistency calibration of LRA. Firstly the power-on  $f_0$  detection can be launched to get the  $f_0$  of LRA. Secondly the waveform frequency stored in SRAM and the  $f_0$  of LRA are used to calculate the code for calibration. Finally the code is written to register 0x5B and the calibration process is end. The  $f_0$  accuracy after LRA consistency calibration is  $\pm 2\text{Hz}$ .

## LRA RESISTANCE DETECT

Software can send command to detect the LRA's resistance. The register RLDET[7:0] report this information. Based on this information host can diagnosis used LRA's status. When RLDET[7:0] is less than low threshold, the LRA is short and if RLDET[7:0] is larger than high threshold, the LRA is open.

## FLEXIBLE HAPTIC DATA PLAYBACK

The device offers multiple ways to playback haptic effects data. The PLAY\_MODE bits select RAM mode, RTP mode or CONT mode. Additional flexibility is provided by the three hardware TRIG pins, which can override PLAY\_MODE bit to playback haptic effects data as configuration.

The device contains 8 kB of integrated SRAM to store customer haptic waveforms' data. The whole SRAM is separated to RAM waveform library and RTP FIFO region by base address. And RAM waveform library is including waveform library version, waveform header and waveform data.

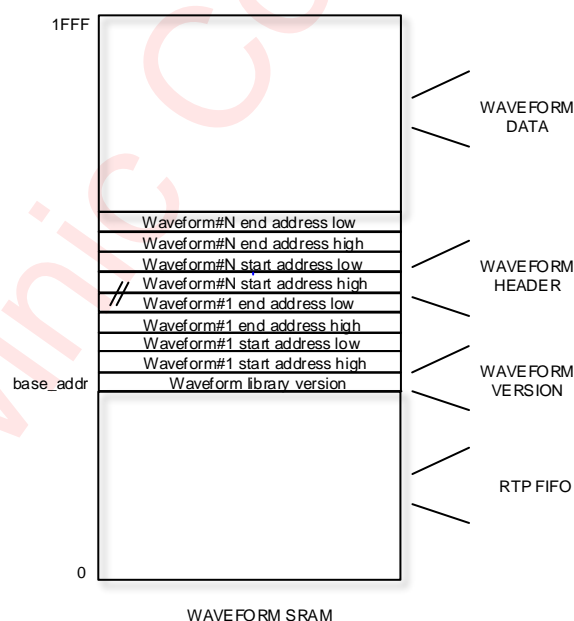


Figure 13 Data Structure in SRAM

SRAM mode and TRIG mode playback the waveforms in RAM waveform library and RTP mode playback the waveform data written in RTP FIFO, CONT mode playback non-filtered or filtered square wave with rated drive voltage .



## RAM WAVEFORM LIBRARY DATA STRUCTURE

A RAM waveform library consists of a waveform version byte, a waveform header section, and the waveform data content. The waveform header defines the data boundaries for each waveform ID in the data field, and the waveform data contains a signed data format (2's complement) to specify the magnitude of the drive.

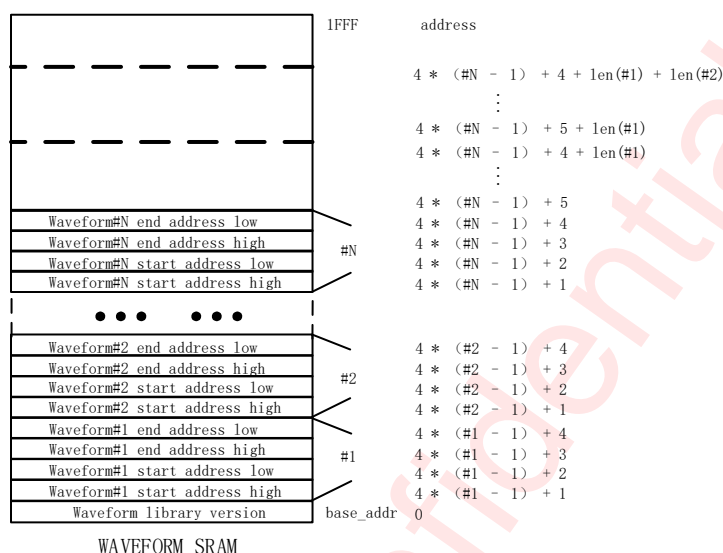


Figure 14 Waveform Library Data Structure

### Waveform Version:

One byte located on SRAM base address, setting to different value to identify different version of RAM waveform library.

### Waveform Header:

The waveform header block consist of N-boundary definition blocks of 4 bytes each. N is the number of waveforms stored in the SRAM (N cannot exceed 127). Each of the boundary definition blocks contain the start address (2 bytes) and end address (2 bytes). So the total length of waveform header block are N\*4 bytes.

The start address contains the location in the memory where the waveform data associated with this waveform begins.

The end address contains the location in the memory where the waveform data associated with this waveform ends.

The waveform ID is determined after base address is defined. Four bytes begins with the address next to base address are the first waveform ID's header, and next four bytes are the second waveform ID's header, and so on.

### Waveform Data:

The waveform data contains a signed data format (2's complement) to specify the magnitude of the drive. The begin address and end address is specified in waveform ID's header.

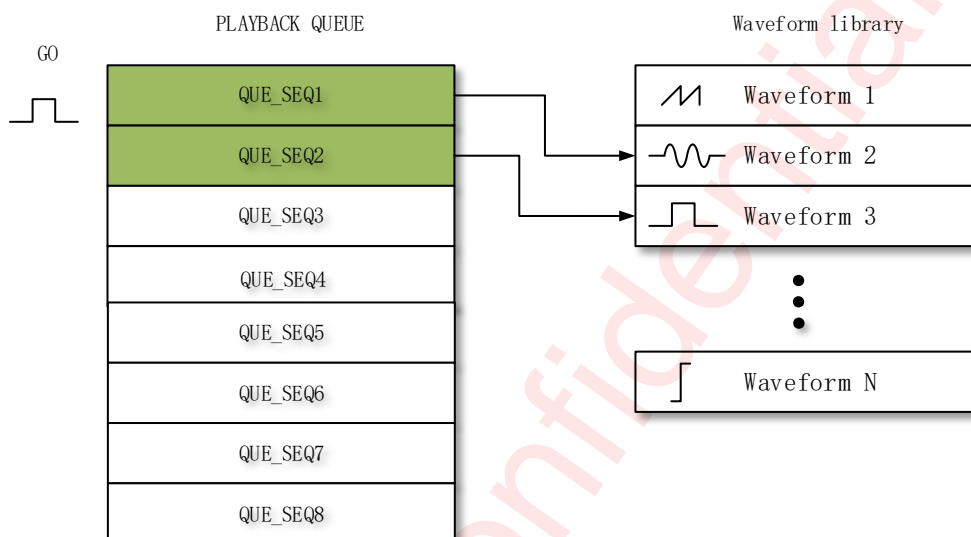
### Waveform Library Initialization Steps:

- Prepare waveform library data including: waveform library version, waveform header fields for waveform in library and waveform data of each waveform;
- Set register 0x04 to 0x63 to let the device in standby mode and enable SRAM initial;

- Set register 0x40, 0x41 to base address;
- Write waveform library data into register 0x42 continually until all the waveform library data written;

## RAM MODE HAPTIC DATA PLAYBACK

To playback haptic data with RAM mode, the waveform ID must first be configured into the waveform playback queue and then the waveform can be played by writing GO bit register.



**Figure 15 RAM Mode Playback**

The waveform playback queue defines waveform IDs in waveform library for playback. Eight QUE\_SEQx registers queue up to eight library waveforms for sequential playback. A waveform ID is an integer value referring to the index of a waveform in the waveform library. Playback begins at QUE\_SEQ1 when the user triggers the waveform playback queue. When playback of that waveform ends, the waveform queue plays the next waveform ID held in QUE\_SEQ2 (if non-zero). The waveform queue continues in this way until the queue reaches an ID value of zero or until all eight IDs are played whichever comes first.

The waveform ID is a 7-bit number. The MSB of each ID register can be used to implement a delay between queue waveforms. When the MSB is high, bits 6-0 indicate the length of the wait time. The wait time for that step then becomes  $QUE\_SEQ[6:0] \times \text{wait\_time unit}$ . Wait\_time unit can be configuration of 20us, 160us, 1280us or 10ms.

The device allows for looping of individual waveforms by using the SEQx\_LOOP registers. When used, the state machine will loop the particular waveform the number of times specified in the associated SEQx\_LOOP register before moving to the next waveform. The waveform-looping feature is useful for long, custom haptic playbacks, such as a haptic ringtone.

### RAM Mode Playback Steps:

- Waveform library must be initialized before playback;
- Set PLAY\_MODE bit to 0 in register 0x04;
- Set playback queue registers (0x07 ~ 0x13) as desired;
- Set STANDBY bit to 0 in register 0x04 to change the device to active mode;
- Set GO bit to 1 in register 0x05 to trigger waveform playback;

- After playback, GO bit will be cleared to 0 and the device will go to standby mode automatically;

### RTP MODE HAPTIC DATA PLAYBACK

The real-time playback mode is a simple, single 8-bit register interface that holds an amplitude value. When real-time playback is enabled, begin to enters a register value to RTP\_DATA over the I<sup>2</sup>C will trigger the playback, the value is played until the data sending finished or removes the device from RTP mode.

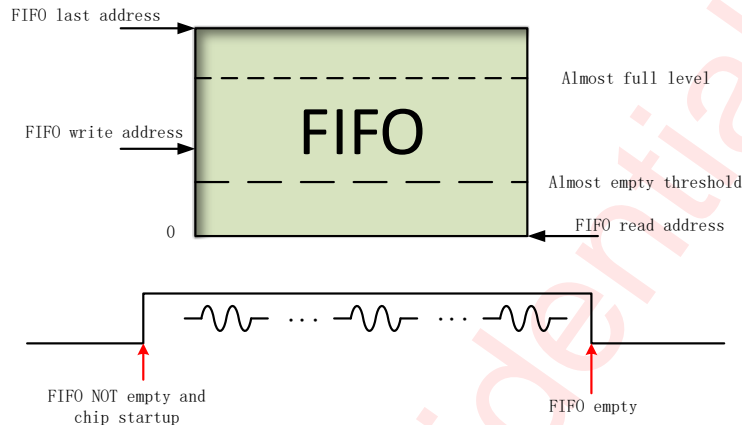


Figure 16 RTP mode playback

#### RTP Mode Playback Steps:

- Prepare RTP data before playback;
- Set PLAY\_MODE bit to 1 in register 0x04;
- Set STANDBY bit to 0 in register 0x04 to change the device to active mode;
- Set GO bit to 1 in register 0x05 to trigger waveform playback;
- Write RTP data continually to register 0x06 to playback RTP waveform;
- HOST need monitor the full and empty status for RTP FIFO;

### TRIG MODE HAPTIC DATA PLAYBACK

The device have three dedicated hardware pins for quickly trigger haptic data playback. Only support edge trigger. Each pin can be configured single edge trigger or double edge trigger. Positive pulse and negative pulse can be supported by configuration.

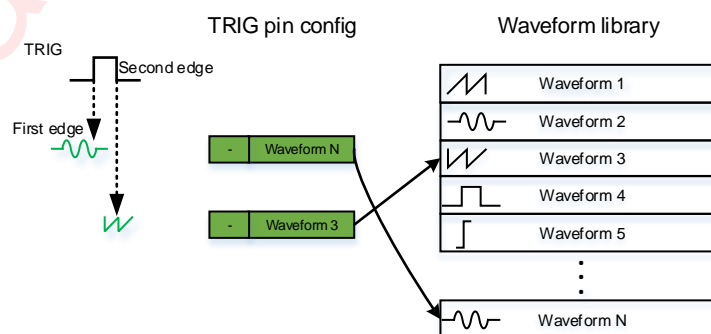


Figure 17 TRIG Mode Playback

Register 0x14 configure the waveform ID for the first edge of TRIG pin 1 and register 0x17 configure the waveform ID for the second edge of TRIG pin 1 if double edge selected by configuring register 0x1B bit 0;

Register 0x15 configure the waveform ID for the first edge of TRIG pin 2 and register 0x18 configure the waveform ID for the second edge of TRIG pin 2 if double edge selected by configuring register 0x1B bit 2;

Register 0x16 configure the waveform ID for the first edge of TRIG pin 3 and register 0x19 configure the waveform ID for the second edge of TRIG pin 3 if double edge selected by configuring register 0x1B bit 4;

Register 0x1B bit 1/bit 3/bit 5 should set to 1 when the trigger signal sent from host is negative pulse.

#### TRIG Mode Playback Steps:

- Waveform library must be initialized before playback;
- Set trigger playback registers (0x14 ~ 0x19, 0x1B) as desired;
- Send trigger ( $\geq 1\mu\text{s}$ ) pulse in TRIG pins to playback waveform.

#### CONT MODE HAPTIC DATA PLAYBACK

The CONT mode mainly performs two functions: power-on f0 detection, real-time resonance-frequency tracking. The power-on f0 detection can be launched when the chip is powered on or a LRA motor's resonant frequency need to be measured. The f0 can be acquired through register 0x68h and register 0x69h. The real-time resonance-frequency tracking function tracks the resonant frequency of a LRA in real time by constantly monitoring the BEMF of the actuator. It provides stronger and more consistent vibrations and lower power consumption. If the resonant frequency shifts for any reason, the function tracks the frequency from cycle to cycle. In addition, a loop-open play mode can be launched for maximum flexibility.

#### Power-On f0 Detection Mode Playback Steps:

- Set PLAY\_MODE bit to 0x2 in register 0x04 to enable CONT mode ;
- Set EN\_F0\_DET bit to 1 in register 0x48 to enable power-on f0 detection;
- Set RC filter function in register 0x2B when using;
- Set power-on f0 detection playback registers (0x48, 0x72, 0x73, 0x7D~0x7F) as desired;
- Set STANDBY bit to 0 in register 0x04 to change the device to active mode;
- Set GO bit to 1 in register 0x05 to trigger waveform playback;
- After playback, GO bit will be cleared to 0 and the device will go to standby mode automatically;
- F0 of the LRA motor can be acquired in register 0x68, 0x69.

#### Real-Time Resonance-Frequency Tracking Mode Playback Steps:

- Set PLAY\_MODE bit to 0x2 in register 0x04 to enable CONT mode;
- Set EN\_F0\_DET bit to 0 and EN\_CLOSE bit to 1 to enable real-time resonance-frequency tracking;
- Set Td in register 0x4B, 0x4C;
- Set RC filter function in register 0x2B when using;
- Set ZC threshold in register 0x72、0x73;
- Set real-time resonance-frequency tracking playback registers (0x48, 0x78~0x7C,) as desired;
- Set brake enable in register 0x48 when using;

- Set STANDBY bit to 0 in register 0x04 to change the device to active mode;
- Set GO bit to 1 in register 0x05 to trigger waveform playback;
- After playback, GO bit will be cleared to 0 and the device will go to standby mode automatically.

**Loop-Open Play Mode Playback Steps:**

- Set PLAY\_MODE bit to 0x2 in register 0x04 to enable CONT mode;
- Set EN\_F0\_DET bit to 0 and EN\_CLOSE bit to 1'b0 to enable loop open play mode;
- Set RC filter function in register 0x2B when using;
- Set loop open playback registers (0x48, 0x79, 0x7B) as desired;
- Set STANDBY bit to 0 in register 0x04 to change the device to active mode;
- Set GO bit to 1 in register 0x05 to trigger waveform playback;
- After playback, GO bit will be cleared to 0 and the device will go to standby mode automatically;

**DC-DC CONVERTER**

The device integrated peak current mode synchronous PWM Boost as H-bridge power stage supply, significantly increase the output voltage dynamic range. Reduces the size of external components and saves PCB space by using about 1.6 MHz switching frequency. Boost output voltage can be set through the I<sup>2</sup>C register 0x34h [7:3]; Boost current limit can be set through register 0x34h [2:0].

The device synchronous Boost with soft-start function to prevent overshoot current at powering-on; integrated the output protection circuit and self-recovery function; integrated Anti-Ring circuit to reduce EMI in DCM mode; built-in substrate switching shutdown circuit, effectively preventing the input and output leakage current anti-irrigation.

**PROTECTION MECHANISMS****OVER VOLTAGE PROTECTION (OVP)**

The boost circuit has integrated the over voltage protection control loop. When the output voltage PVDD is above the threshold, the boost circuits will stop working, until the voltage of PVDD going down and under the normal fixed working voltage.

**OVER TEMPERATURE PROTECTION (OTP)**

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 160°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130°C), the output stages will start to operate normally again.

**OVER CURRENT (SHORT) PROTECTION (OCP)**

The short circuit protection function is triggered when HDP/HDN is short too PVDD/GND or HDP is short to HDN, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

## VBAT UNDER VOLTAGE LOCK OUT PROTECTION (UVLO)

The device has a battery monitor that monitors the VBAT level to ensure that is above threshold 2.8V, In the event of a VBAT droop, the device immediately power down the Boost and H-bridge driver and latches the UVLO flag.

## DRIVE DATA ERROR PROTECTION (DDEP)

When haptic data sent to drive LRA is error such as: a DC data or almost DC data, it will cause the LRA heat to brake. The device configurable immediately power down the Boost and H-bridge driver and latched the DDEP flag.

## I<sup>2</sup>C INTERFACE

This device supports the I<sup>2</sup>C serial bus and data transmission protocol in fast mode at 400kHz and super-fast mode at 1000kHz. This device operates as a slave on the I<sup>2</sup>C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 2.2kΩ. This device can support different high level (1.8V~3.3V) of this I<sup>2</sup>C interface.

## DEVICE ADDRESS

The I<sup>2</sup>C device address (7-bit) can be set using the AD pin according to the following table:

Table 3 Address Selection

AD	I <sup>2</sup> C address (7-bit)
0	0x5A
1	0x5B

## DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

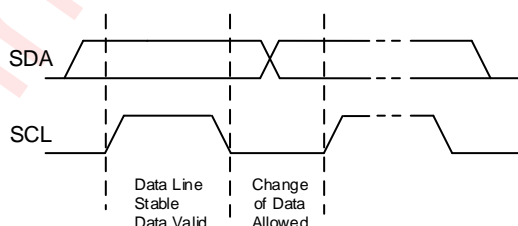


Figure 18 Data Validation Diagram

## GENERAL I<sup>2</sup>C OPERATION

The I<sup>2</sup>C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguish master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.

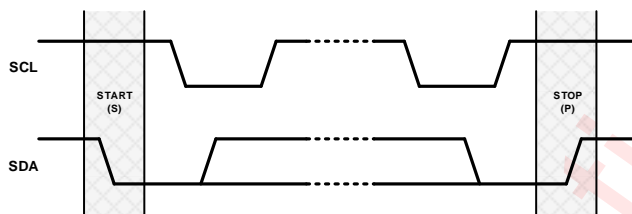
SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL default is a high level. There is no limit on the number of bytes that can be transmitted between start and stop

conditions. When the last word transfers, the master generates a stop condition to release the bus.

START state: The SCL maintain a high level, SDA from high to low level

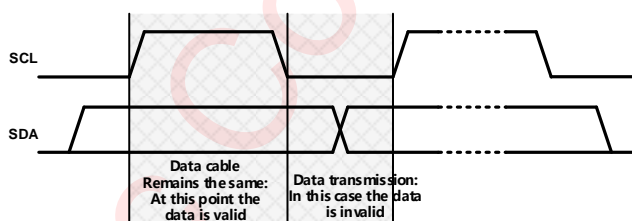
STOP state: The SCL maintain a high level, SDA pulled low to high level

Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in Figure 19.



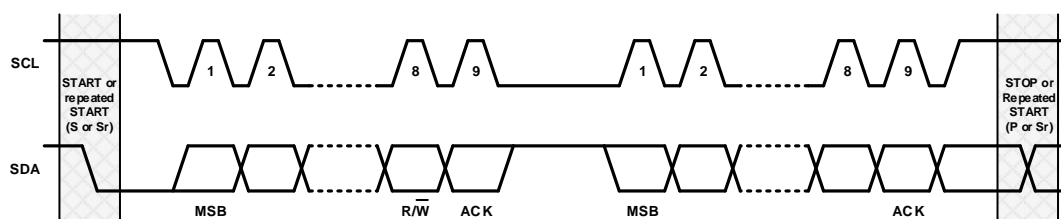
**Figure 19 START And STOP State Generation Process**

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in Figure 20. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an confirmation bit (Acknowledge, ACK or A ), as shown in Figure 21. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits data are confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of data can be transferred between START and STOP state.



**Figure 20 The Data Transfer Rules on The I²C Bus**

The whole process of actual data transmission is shown in Figure 21. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag ( $\overline{R/W}$ ). The flag is used to specify the direction of transmission of subsequent data. The master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.



**Figure 21 Data Transmission on The I²C Bus**



## WRITE PROCESS

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, the device as the slave device, the transmission process in accordance with the following steps, as shown in Figure 22:

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag  $R/\overline{W} = 0$ );

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit register address to which the first data byte will written;

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data by sending another pair of data bytes, just need to repeat the sequence from step 6. In the latter case, the targeted register address will have been auto-incremented by the device.

The master device generates the STOP state to end the data transmission.

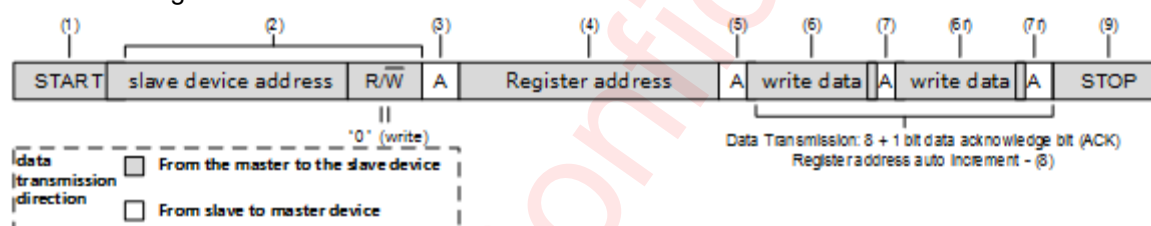


Figure 22 Writing Process (Data Transmission Direction Remains The Same)

## READ PROCESS

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, the device as the slave device, the transmission process carried out by following steps listed in Figure 23:

Master device asserts a start condition;

Master device transmits the 7 bits address of the device, and followed by a "read / write" flag ( $R/\overline{W} = 1$ );

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the register address to make sure where the first data byte will read;

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START;

Master sends 7-bits address of the slave device and followed by a read / write flag (flag  $R/\overline{W} = 1$ ) again;

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

Master transmits 8 bits of data to register which needs to be read;

The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

The device automatically increment register address once after sent each acknowledge bit (ACK),

The master device generates the STOP state to end the data transmission.



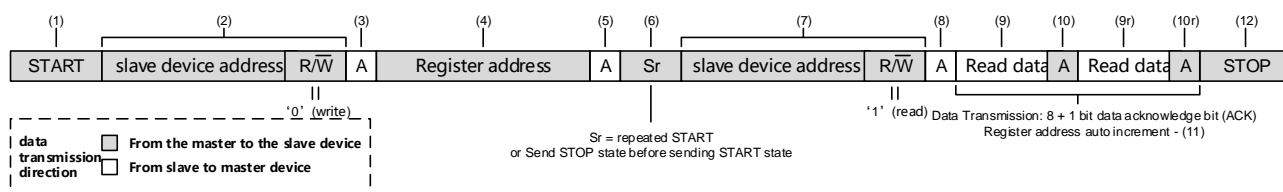


Figure 23 Reading Process (Data Transmission Direction Remains The Same)

## REGISTER CONFIGURATION

## REGISTER LIST

ADDR	NAME									Default
		7	6	5	4	3	2	1	0	
0x00	ID	CHIPID								0x97
0x01	SYSST	BSTERRS	OVS	UVLS	FF_AES	FF_AFS	OCDS	OTS	DONES	0x10
0x02	SYSINT	BSTERRI	OVI	UVLI	FF_AEI	FF_AFI	OCDI	OTI	DONEI	0x10
0x03	SYSINTM	BSTERRM	OVM	UVLM	FF_AEM	FF_AFM	OCDM	OTM	DONEM	0x7F
0x04	SYSCTRL	WAVDAT_MODE		EN_RAMINIT	Reserved	PLAY_MODE		BST_MODE	STANDBY	0x43
0x05	GO	Reserved							GO	0x00
0x06	RTPDATA	RTP_DATA								0x00
0x07	WAVSEQ1	WAIT1	WAV_FRM_SEQ1							0x01
0x08	WAVSEQ2	WAIT2	WAV_FRM_SEQ2							0x00
0x09	WAVSEQ3	WAIT3	WAV_FRM_SEQ3							0x00
0x0A	WAVSEQ4	WAIT4	WAV_FRM_SEQ4							0x00
0x0B	WAVSEQ5	WAIT5	WAV_FRM_SEQ5							0x00
0x0C	WAVSEQ6	WAIT6	WAV_FRM_SEQ6							0x00
0x0D	WAVSEQ7	WAIT7	WAV_FRM_SEQ7							0x00
0x0E	WAVSEQ8	WAIT8	WAV_FRM_SEQ8							0x00
0x0F	WAVLOOP1	SEQ1_LOOP				SEQ2_LOOP				0x00
0x10	WAVLOOP2	SEQ3_LOOP				SEQ4_LOOP				0x00
0x11	WAVLOOP3	SEQ5_LOOP				SEQ6_LOOP				0x00
0x12	WAVLOOP4	SEQ7_LOOP				SEQ8_LOOP				0x00
0x13	MAINLOOP	Reserved				MAINLOOP				0x00
0x14	TRG1SEQP	Reserved	TRG1_FRM_SEQ_P							0x01
0x15	TRG2SEQP	Reserved	TRG2_FRM_SEQ_P							0x01
0x16	TRG3SEQP	Reserved	TRG3_FRM_SEQ_P							0x01
0x17	TRG1SEQN	Reserved	TRG1_FRM_SEQ_N							0x01
0x18	TRG2SEQN	Reserved	TRG2_FRM_SEQ_N							0x01
0x19	TRG3SEQN	Reserved	TRG3_FRM_SEQ_N							0x01
0x1B	TRGCFG1	Reserved		TRG3_POLAR	TRG3_EDGE	TRG2_POLAR	TRG2_EDGE	TRG1_POLAR	TRG1_EDGE	0x00
0x1C	TRGCFG2	Reserved					TRG3_EN	TRG2_EN	TRG1_EN	0x40
0x20	DBGCTRL	Reserved				INTMODE		WAITSLOT		0xA0
0x21	BASE_ADDRH	Reserved			BASE_ADDRH					0x08
0x22	BASE_ADDRL	BASE_ADDRL								0x00
0x23	FIFO_AEH	Reserved				FIFO_AEH				0x02
0x24	FIFO_AEL	FIFO_AEL								0x00
0x25	FIFO_AFH	Reserved				FIFO_AFH				0x06
0x26	FIFO_AFL	FIFO_AFL								0x00
0x2B	DATCTRL	Reserved		EN_LPF	INTP	Reserved		EN_FIR	Reserved	0x40
0x2D	PWMPRC	PRC_EN	PRCTIME							0xA0
0x2E	PWMDBG	Reserved	PWMCLK_MODE		PD_HWM	Reserved			PWM_OE	0xC1
0x30	DBGSTAT	LDO_OK	BST_SCP	BST_OVP	VBGOK	Reserved	FF_ERROR	FF_FULL	FF_EMPTY	0x01
0x34	BSTCFG	Reserved					BST_MAX_PEAK_CUR			0x05
0x39	DATDBG	GAIN								0x80
0x3A	BSTDBG4	Reserved		BST_VO					Reserved	0x62

0x3E	PRLVL	PR_EN	PRLVL						0xBF	
0x3F	PRTIME	PRTIME							0x12	
0x40	RAMADDRH	Reserved			RAMADDRH				0x00	
0x41	RAMADDRL	RAMADDRL							0x00	
0x42	RAMDATA	RAMDATA							0x00	
0x48	CONT_CTRL	Reserved	FLAG_WAIT		CONT_MODE	EN_CLOSE	EN_F0_DET	Reserved	EN_AUTO_BRK	0x99
0x49	F_PRE_H	F_PRE_H							0x07	
0x4A	F_PRE_L	F_PRE_L							0x25	
0x4B	TD_H	Reserved			TD_H				0x00	
0x4C	TD_L	TD_L							0x5D	
0x5F	DETCTRL	Reserved	RL_OS	PRCT_MODE	Reserved		VBAT_GO	DIAG_GO	0x00	
0x60	RLDET	RL							0x00	
0x61	OSDET	OS							0x80	
0x62	VBATDET	VBAT							0x00	
0x66	ADCTEST	Reserved	VBAT_MODE	Reserved					0x00	
0x68	F_LRA_F0_H	F_LRA_F0_H							0x00	
0x69	F_LRA_F0_L	F_LRA_F0_L							0x00	
0x6A	F_LRA_CONT_H	F_LRA_CONT_H							0x00	
0x6B	F_LRA_CONT_L	F_LRA_CONT_L							0x00	
0x72	ZC_THRSH_H	ZC_THRSH_H							0x0F	
0x73	ZC_THRSH_L	ZC_THRSH_L							0xF1	
0x78	BEMF_NUM	Reserved			NUM_BRK				0x53	
0x79	DRV_TIME	DRV_TIME							0x3F	
0x7A	TIME_NZC	TIME_NZC							0x1F	
0x7B	DRV_LVL	DRV_LEVEL							0x50	
0x7C	DRV_LVL_OV	DRV_LEVEL_OV							0x7F	
0x7D	NUM_F0_1	NUM_F0_PRE			Reserved				0x59	
0x7E	NUM_F0_2	NUM_F0_REPEAT							0x05	
0x7F	NUM_F0_3	NUM_F0_TRACE							0x0F	

## REGISTER DETAILED DESCRIPTION

## ID: Chip ID Register(Address 0x00)

Bit	Symbol	R/W	Description	Default
7:0	CHIPID	RO	Chip ID (0x97) will be returned after read. All configuration registers will be reset to default value after 0xaa is written	0x97

## SYSST: System Status Register(Address 0x01) Default: 0x10

Bit	Symbol	R/W	Description	Default
7	BSTERRS	RO	Boost scp/ovp error	0
6	OVS	RO	Wave data overflow or DPWM DC error	0
5	UVLS	RO	Under voltage lock out signal, 0: VDD>UVLO_THRES 1: VDD<UVLO_THRES	0
4	FF_AES	RO	1: RTP FIFO almost empty	1
3	FF_AFS	RO	1: RTP FIFO almost full	0
2	OCDS	RO	1: Over current status	0
1	OTS	RO	1: Over temperature status	0
0	DONES	RO	The indication of playback done	0

## SYSINT: System Interrupt Register(Address 0x02) Default: 0x10

Bit	Symbol	R/W	Description	Default
7	BSTERRI	RC	Interrupt for boost scp/ovp error	0
6	OVI	RC	Interrupt for OVS	0
5	UVLI	RC	Interrupt for UVLS	0
4	FF_AEI	RC	Interrupt for FF_AES	1
3	FF_AFI	RC	Interrupt for FF_AFS	0
2	OCDI	RC	Interrupt for OCDS	0
1	OTI	RC	Interrupt for OTS	0
0	DONEI	RC	Interrupt for DONES	0

## SYSINTM: System Interrupt Mask Register(Address 0x03) Default: 0x7F

Bit	Symbol	R/W	Description	Default
7	BSTERRM	RW	Interrupt mask for boost scp/ovp error	0
6	OVM	RW	Interrupt mask for OVI	1
5	UVLM	RW	Interrupt mask for UVLI	1
4	FF_AEM	RW	Interrupt mask for FF_AEI	1
3	FF_AFM	RW	Interrupt mask for FF_AFI	1
2	OCDM	RW	Interrupt mask for OCDI	1
1	OTM	RW	Interrupt mask for OTI	1
0	DONEM	RW	Interrupt mask for DONEI	1

**SYCTRL: System Control Register(Address 0x04) Default: 0x43**

Bit	Symbol	R/W	Description	Default
7:6	WAVDAT_MODE	RW	Waveform data upsample rate selection: 1: 1x upsample rate 0: 2x upsample rate others: 4x upsample rate	0x1
5	EN_RAMINIT	RW	Enable SRAM initialization for effects After power on, system should initial SRAM for preload effects, to do so, this bit must be set to 1	0
4	Reserved	RW	Reserved	
3:2	PLAY_MODE	RW	Waveform play mode for GO trig 0: RAM mode 1: RTP mode 2: CONT mode	0x0
1	BST_MODE	RW	BOOST mode 0: Bypass mode 1: BOOST mode(default)	1
0	STANDBY	RW	Chip enable/disable control 0: set chip into active mode 1: set chip into standby mode	1

**GO: Process Control Register(Address 0x05) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:1	Reserved	RWC	Reserved	
0	GO	RWC	RAM/RTP/CONT mode playback trig bit When set to 1, chip will playback waveforms from SRAM as configuration, after playback finished , it will be cleared internally During playback, if it is set to 0, playback will stop	0

**RTPDATA: RTP Mode Data Register(Address 0x06) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:0	RTP_DATA	RW	RTP mode, data write entry, when data written into this register, the data will be written into RTP FIFO	0

**WAVSEQ1 : First Waveform Register(Address 0x07) Default: 0x01**

Bit	Symbol	R/W	Description	Default
7	WAIT1	RW	When set to 1, WAV_FRM_SEQ1 means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ1	RW	Wait time or wave sequence number	0x01

**WAVSEQ2: Second Waveform Register(Address 0x08) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7	WAIT2	RW	When set to 1 , WAV_FRM_SEQ2 means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ2	RW	Wait time or wave sequence number	0x00

**WAVSEQ3: Third waveform Register(Address 0x09) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7	WAIT3	RW	When set to 1, WAV_FRM_SEQ3 means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ3	RW	Wait time or wave sequence number	0x00

**WAVSEQ4: Fourth Waveform Register(Address 0x0A) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7	WAIT4	RW	When set to 1, WAV_FRM_SEQ4 means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ4	RW	Wait time or wave sequence number	0x00

**WAVSEQ5: Fifth Waveform Register(Address 0x0B) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7	WAIT5	RW	When set to 1, WAV_FRM_SEQ5 means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ5	RW	Wait time or wave sequence number	0x00

**WAVSEQ6: Sixth Waveform Register(Address 0x0C) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7	WAIT6	RW	When set to 1, WAV_FRM_SEQ6 means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ6	RW	Wait time or wave sequence number	0x00

**WAVSEQ7: Seventh Waveform Register(Address 0x0D) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7	WAIT7	RW	When set to 1, WAV_FRM_SEQ7 means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ7	RW	Wait time or wave sequence number	0x00

**WAVSEQ8: Eighth Waveform Register(Address 0x0E) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7	WAIT8	RW	When set to 1, WAV_FRM_SEQ8 means wait time, else means wave sequence number	0
6:0	WAV_FRM_SEQ8	RW	Wait time or wave sequence number	0x00

**WAVLOOP1: Waveform Loop Control Register(Address 0x0F) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:4	SEQ1_LOOP	RW	Control the loop number of the first sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0
3:0	SEQ2_LOOP	RW	Control the loop number of the second sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0

**WAVLOOP2: Waveform Loop Control Register(Address 0x10) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:4	SEQ3_LOOP	RW	Control the loop number of the third sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0
3:0	SEQ4_LOOP	RW	Control the loop number of the fourth sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0

**WAVLOOP3: Waveform Loop Control Register(Address 0x11) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:4	SEQ5_LOOP	RW	Control the loop number of the fifth sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0

3:0	SEQ6_LOOP	RW	Control the loop number of the sixth sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0
-----	-----------	----	--	-----

**WAVLOOP4: Waveform Loop Control Register(Address 0x12) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:4	SEQ7_LOOP	RW	Control the loop number of the seventh sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0
3:0	SEQ8_LOOP	RW	Control the loop number of the eighth sequence 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0

**MAINLOOP : Main Loop Control Register(Address 0x13) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Reserved	
3:0	MAINLOOP	RW	Control the main loop number 0000~1110: play n+1 time 1111: playback infinitely until GO set to 0	0x0

**TRG1SEQP: TRIG1 First Edge Waveform Register(Address 0x14) Default: 0x01**

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	
6:0	TRG1_FRM_SEQ_P	RW	Wave sequence number triggered by first edge of trig1 pulse	0x01

**TRG2SEQP: TRIG2 First Edge Waveform Register(Address 0x15) Default: 0x01**

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	
6:0	TRG2_FRM_SEQ_P	RW	Wave sequence number triggered by first edge of trig2 pulse	0x01

**TRG3SEQP: TRIG3 First Edge Waveform Register(Address 0x16) Default: 0x01**

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	
6:0	TRG3_FRM_SEQ_P	RW	Wave sequence number triggered by first edge of trig3 pulse	0x01

**TRG1SEQN: TRIG1 Second Edge Waveform Register(Address 0x17) Default: 0x01**

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	
6:0	TRG1_FRM_SEQ_N	RW	Wave sequence number triggered by second edge of trig1 pulse	0x01

**TRG2SEQN: TRIG2 Second Edge Waveform Register(Address 0x18) Default: 0x01**

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	
6:0	TRG2_FRM_SEQ_N	RW	Wave sequence number triggered by second edge of trig2 pulse	0x01

**TRG3SEQN: TRIG3 Second Edge Waveform Register(Address 0x19) Default: 0x01**

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	

6:0	TRG3_FRM_SEQ_N	RW	Wave sequence number triggered by second edge of trig3 pulse	0x01
-----	----------------	----	--	------

**TRGCFG1: Trig Pins Config Register(Address 0x1B) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Reserved	
5	TRG3_POLAR	RW	TRIG3 pin active polarity, when host supply positive pulse, this bit set to 0, else set to 1	0
4	TRG3_EDGE	RW	TRIG3 pin triggering edge config, set to 1 , only first edge can trig playback, else both edge can trig playback	0
3	TRG2_POLAR	RW	TRIG2 pin active polarity, when host supply positive pulse, this bit set to 0, else set to 1	0
2	TRG2_EDGE	RW	TRIG2 pin triggering edge config, set to 1 , only first edge can trig playback, else both edge can trig playback	0
1	TRG1_POLAR	RW	TRIG1 pin active polarity, when host supply positive pulse, this bit set to 0, else set to 1	0
0	TRG1_EDGE	RW	TRIG1 pin triggering edge config, set to 1 , only first edge can trig playback, else both edge can trig playback	0

**TRGCFG2: Trig Pins Config Register(Address 0x1C) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:3	Reserved	RW	Reserved	
2	TRG3_EN	RW	TRIG3 pin triggering enable	0
1	TRG2_EN	RW	TRIG2 pin triggering enable	0
0	TRG1_EN	RW	TRIG1 pin triggering enable	0

**DBGCTRL: Debug Control Register(Address 0x20) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Reserved	
3:2	INTMODE	RW	Interrupt mode x0: interrupt level mode; x1: interrupt edge mode; 0x: interrupt posedge mode; 1x: interrupt both edge mode;	0x0
1:0	WAITSLOT	RW	Unit of wait time (upsample rate determined by WAVDAT_MODE register) 00: (1/PWMCLK_MODE)*upsample rate 01: (8/PWMCLK_MODE)*upsample rate 10: (64/PWMCLK_MODE)*upsample rate 11: (512/PWMCLK_MODE)*upsample rate	0x0

**BASE\_ADDRH: High Five Bits of Wave SRAM Register(Address 0x21) Default: 0x08**

Bit	Symbol	R/W	Description	Default
7:5	Reserved		Reserved	
4:0	BASE_ADDRH	RW	High five bits of start Address of wave SRAM	0x08

**BASE\_ADDRL: Low Eight Bits of Wave SRAM Register(Address 0x22) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:0	BASE_ADDRL	RW	Low eight bits of start Address of wave SRAM	0x00

**FIFO\_AEH: High Four Bits of FIFO AE Register(Address 0x23) Default: 0x02**

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Reserved	



3:0	FIFO_AEH	RW	High four bits of RTP FIFO almost empty threshold	0x2
-----	----------	----	---	-----

**FIFO\_AEL: Low Eight Bits of FIFO AE Register(Address 0x24) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:0	FIFO_AEL	RW	Low eight bits of RTP FIFO almost empty threshold	0x00

**FIFO\_AFH: High Four Bits of FIFO AF Register(Address 0x25) Default: 0x06**

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Reserved	
3:0	FIFO_AFH	RW	High four bits of RTP FIFO almost full threshold	0x6

**FIFO\_AFL: Low Eight Bits of FIFO AF Register(Address 0x26) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:0	FIFO_AFL	RW	Low eight bits of RTP FIFO almost full threshold	0x00

**DATCTRL: Global Control Data Register(Address 0x2B) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Reserved	
5	EN_LPF	RW	Set enable of RC filter	0
4	INTP	RW	Interrupt pin polarity: 0: low active 1: high active	0
3:2	Reserved	RW	Reserved	
1	EN_FIR	RW	Set enable of FIR filter	0
0	Reserved	RW	Reserved	

**PWMPRC: PWM Output Protect Configuration Register(Address 0x2D) Default: 0xA0**

Bit	Symbol	R/W	Description	Default
7	PRC_EN	RW	Set enable of output signal protection mode of pwm	1
6:0	PRCTIME	RW	Set protection time of output signal protection mode of pwm	0x20

**PWMDBG: PWM Debug Register(Address 0x2E) Default: 0xC1**

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	
6:5	PWMCLK_MODE	RW	PWM data sample rate mode: 0x: 48kB 10: 24kB 11: 12kB	0x2
4	PD_HWM	RW	Shutdown half wave modulate	0
3:1	Reserved	RW	Reserved	
0	PWMOE	RW	PWM output enable	1

**DBGSTAT: Debug Status Register(Address 0x30) Default: 0x81**

Bit	Symbol	R/W	Description	Default
7	LDO_OK	RO	LDO OK indication	1
6	BST_SCP	RO	BOOST short current protect status	0
5	BST_OVP	RO	BOOST OVP status	0
4	VBGOK	RO	VBG OK indication	0

3	Reserved	RO	Reserved	
2	FF_ERROR	RO	RTP FIFO error status	0
1	FF_FULL	RO	RTP FIFO full status	0
0	FF_EMPTY	RO	RTP FIFO empty status	1

**BSTCFG: Boost Config Register(Address 0x34) Default: 0x05**

Bit	Symbol	R/W	Description	Default
7:3	Reserved	RW	Reserved	
2:0	BST_MAX_PEA_CUR	RW	Boost maxim inductor peak current: 000: 1.75A 001: 2A 010: 2.25A 011: 2.5A 100: 3A 101: 3.5A 110: 3.75A 111: 4A	0x5

**DATDBG: Data Gain Register(Address 0x39) Default: 0x80**

Bit	Symbol	R/W	Description	Default
7:0	GAIN	RW	Gain setting for waveform data, it is a global setting for waveform data of RAM/RTP/TRG	0x80

**BSTDBG4: Boost Debug Register 4(Address 0x3A) Default: 0x62**

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Reserved	
5:1	BST_VO	RW	PVDD output voltage setting, default is 10001: 8.41V 00000: 6V 00001: 6V+142mV*1 00010: 6V+142mV*2 ..... 11111: 6V+142mV*31	0x11
0	Reserved	RW	Reserved	

**PRLVL: Waveform Protect Level Configuration(Address 0x3E) Default: 0xBF**

Bit	Symbol	R/W	Description	Default
7	PR_EN	RW	Set enable of input signal protection mode of pwm	1
6:0	PRLVL	RW	Set protection voltage of input signal protection mode of pwm	0x3F

**PRTIME: Waveform Protect Period Configuration(Address 0x3F) Default: 0x12**

Bit	Symbol	R/W	Description	Default
7:0	PRTIME	RW	Set protection time of input signal protection mode of pwm	0x12

**RAMADDRH: SRAM Address 0xhigh Register(Address 0x40) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RW	Reserved	
4:0	RAMADDRH	RW	SRAM Address 0xhigh five bits	0x00

**RAMADDRL: SRAM Address 0xlow Register(Address 0x41) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:0	RAMADDRL	RW	SRAM Address 0xlow eight bits	0x00

**RAMDATA: SRAM Data Register(Address 0x42) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:0	RAMDATA	RW	SRAM data entry	0x00

**CONT\_CTRL: CONT Mode Control Register(Address 0x48) Default: 0x99**

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	
6:5	FLAG_WAIT	RW	The number of BEMF period for measure 2'b00/2'b11: one period 2'b01: two periods 2'b10: four periods	0x0
4	CONT_MODE	RW	Playback time control 1:control by register iRtime 0:control by go_signal	1
3	EN_CLOSE	RW	Loop_close play mode enable 1:loop_close play mode 0:loop_open play mode	1
2	EN_F0_DET	RW	Power_on f0 detection mode enable 1:enable 0:disable	0
1	Reserved	RW	Reserved	
0	EN_AUTO_BRK	RW	Autobrake enable 1:enable 0:disable	1

**F\_PRE\_H: High 8 Bits Pre Setting f0 Value(Address 0x49) Default: 0x07**

Bit	Symbol	R/W	Description	Default
7:0	F_PRE_H	RW	High eight bits of default value for the f0 of LRA. $F\_PRE = \{F\_PRE\_H, F\_PRE\_L\} \times 2.6\mu s$	0x07

**F\_PRE\_L: Low 8 Bits Pre Setting f0 Value(Address 0x4A) Default: 0x25**

Bit	Symbol	R/W	Description	Default
7:0	F_PRE_L	RW	Low eight bits of default value for the f0 of LRA. $F\_PRE = \{F\_PRE\_H, F\_PRE\_L\} \times 2.6\mu s$	0x25

**TD\_H: High 4 Bits of Delay Time Setting(Address 0x4B) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Reserved	
3:0	TD_H	RW	High four bits of the time delay $TD = \{TD\_H, TD\_L\} \times 2.6\mu s$	0x0

**TD\_L: Low 8 Bits of Delay Time Setting(Address 0x4C) Default: 0x5D**

Bit	Symbol	R/W	Description	Default
7:0	TD_L	RW	Low eight bits of the time delay $TD = \{TD\_H, TD\_L\} \times 2.6\mu s$	0x5D

**DETCTRL: Detection Control Register(Address 0x5F) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	
6	RL_OS	RW	Set diagnostic mode 1: RL detection of actuator 0: OS detection of ADC	0
5	PRCT_MODE	RW	Set protect mode 0: valid 1: invalid	0
4:2	Reserved	RW	Reserved	
1	VBAT_GO	RW	Set enabled of VBAT mode	0
0	DIAG_GO	RW	Set enabled of DIAG mode	0

**RLDET: Detected RL of LRA Register(Address 0x60) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:0	RL	RO	Measured resistance value of LRA in DIAG mode	0x00

**OSDET: Detected Offset of LRA Register(Address 0x61) Default: 0x80**

Bit	Symbol	R/W	Description	Default
7:0	OS	RO	Measured OS value in OS mode	0x80

**VBATDET: Detected VBAT Register(Address 0x62) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:0	VBAT	RO	Measured VBAT value in VBAT mode	0x00

**ADCTEST: ADC Test Register(Address 0x66) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Reserved	
6	VBAT_MODE	RW	VBAT adjust mode 0: software adjust mode 1: hardware adjust mode	0
5:0	Reserved	RW	Reserved	

**F\_LRA\_F0\_H: High 8 Bits Detected f0 Value(Address 0x68) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:0	F_LRA_F0_H	RW	High eight bits of the measure value of f0 in the f0 detection mode $F\_LRA\_F0 = \{F\_LRA\_F0\_H, F\_LRA\_F0\_L\} \times 2.6\mu s$	0x00

**F\_LRA\_F0\_L: Low 8 Bits Detected f0 Value(Address 0x69) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:0	F_LRA_F0_L	RW	Low eight bits of the measure value of f0 in the f0 detection mode $F\_LRA\_F0 = \{F\_LRA\_F0\_H, F\_LRA\_F0\_L\} \times 2.6\mu s$	0x00

**F\_LRA\_CONT\_H: High 8 Bits CONT\_ENG Gotten f0 Value(Address 0x6A) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:0	F_LRA_CONT_H	RW	High eight bits of the measure value of f0 in the continuous detection mode $F\_LRA\_CONT = \{F\_LRA\_CONT\_H, F\_LRA\_CONT\_L\} \times 2.6\mu s$	0x00

**F\_LRA\_CONT\_L: Low 8 Bits CONT\_ENG Gotten f0 Value(Address 0x6B) Default: 0x00**

Bit	Symbol	R/W	Description	Default
7:0	F_LRA_CONT_L	RW	Low eight bits of the measure value of f0 in the continuous detection mode F_LRA_CONT = {F_LRA_CONT_H,F_LRA_CONT_L} x 2.6us	0x00

**ZC\_THRSH\_H: Zero Cross Threshold High 8 Bits Configuration Register(Addr 0x72) Default: 0x0F**

Bit	Symbol	R/W	Description	Default
7:0	ZC_THRSH_H	RW	Zero-cross detection positive threshold of BEMF	0x0F

**ZC\_THRSH\_L: Zero Cross Threshold Low 8 Bits Configuration Register(Addr 0x73) Default: 0xF1**

Bit	Symbol	R/W	Description	Default
7:0	ZC_THRSH_L	RW	Zero-cross detection negative threshold of BEMF	0xF1

**BEMF\_NUM: BEMF Detection Cycles Configuration Register(Addr 0x78) Default: 0x53**

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Reserved	
3:0	NUM_BRK	RW	Number of pulse for braking	0x3

**DRV\_TIME: Drive Time Setting Register(Address 0x79) Default: 0x3F**

Bit	Symbol	R/W	Description	Default
7:0	DRV_TIME	RW	Set play time of real-time resonance-frequency tracking mode or loop-open play mode. Drive time = DRV_TIME x 666.67us	0x3F

**TIME\_NZC: Non Zero Cross Time Setting Register(Address 0x7A) Default: 0x1F**

Bit	Symbol	R/W	Description	Default
7:0	TIME_NZC	RW	Set time threshold of non-zero-cross. NZC time = TIME_NZC x 166.67us	0x1F

**DRV\_LVL: Drive Level Setting Register(Address 0x7B) Default: 0x50**

Bit	Symbol	R/W	Description	Default
7:0	DRV_LVL	RW	Set the level of drive waveform in normal driving	0x50

**DRV\_LVL\_OV: Drive Level for Overdrive Setting Register(Address 0x7C) Default: 0x7F**

Bit	Symbol	R/W	Description	Default
7:0	DRV_LVL_OV	RW	Set the level of drive waveform in overdrive	0x7F

**NUM\_F0\_1: Number Configuration for F0 Trace Register 1 (Addr 0x7D) Default: 0x59**

Bit	Symbol	R/W	Description	Default
7:4	NUM_F0_PRE	RW	Drive waveform play times in the first period in the f0 detection	0x5
3:0	Reserved	RW	Reserved	

**NUM\_F0\_2: Number Configuration for F0 Trace Register 2 (Address 0x7E) Default: 0x05**

Bit	Symbol	R/W	Description	Default
7:0	NUM_F0_REPEAT	RW	Repeat times in the f0 detection	0x05

**NUM\_F0\_3: Number Configuration for F0 Trace Register 3 (Address 0x7F) Default: 0x0F**

Bit	Symbol	R/W	Description	Default
7:0	NUM_F0_TRACE	RW	Drive waveform play times in the second period and later in the f0 detection	0x0F

awinic Confidential

## APPLICATION INFORMATION

### INDUCTOR SELECTION GUIDELINE

Selecting inductor needs to consider Inductance, size, magnetic shielding, saturation current and temperature current.

#### a) Inductance

Inductance value is limited by the boost converter's internal loop compensation. In order to ensure phase margin sufficient under all operating conditions, recommended 1μH inductor.

#### b) Size

For a certain value of inductor, the smaller the size, the greater the parasitic series resistance of the inductor DCR, the higher the loss, corresponds to the lower efficiency.

#### c) Magnetic shielding

Magnetic shielding can effectively prevent the inductance of the electromagnetic radiation interference. It is much better to choose inductance with magnetic shielding in the application of EMI sensitive environment.

#### d) Saturation current and temperature rise of current

Inductor saturation current and temperature rise current value are important basis for selecting the inductor. As the inductor current increases, on the one hand, since the magnetic core begins to saturate, inductance value will decline; on the other hand, the inductor's parasitic resistance inductance and magnetic core loss can lead to temperature rise. In general, the current value is defined as the saturation current  $I_{SAT}$  when the inductance value drops to 70%; the current value is defined as temperature rise current  $I_{RMS}$  when inductance temperature rise 40°C.

For particular applications, need to calculate the maximum  $I_{L\_PEAK}$  and  $I_{L\_RMS}$ , which is a basis of selecting the inductor. When  $V_{BAT}=3.8V$ ,  $PVDD=8.5V$ ,  $R_L=8\Omega$ , Output drive  $2 \times R_{DS(on)}=350m\Omega$ , when the maximum power without distortion, the output power is calculated as follows:

$$P_{OUT} = \frac{\left( V_{OUT} \times \frac{R_L}{R_L + 2 \times R_{DS(on)}} \right)^2}{2 \times R_L \times (1 - 2.3\%)} = \frac{\left( 8.5 \times \frac{8}{8 + 0.35} \right)^2}{2 \times 8 \times 0.977} W = 4.242 W$$

Where the coefficients in the denominator of (0.977) is the power ratio of no truncation maximum output. In such a large output power, the overall efficiency of the output drive is typically 80%, in order to calculate the maximum average current  $I_{MAX\_AVG\_VDD}$  and maximum peak current  $I_{MAX\_PEAK\_VDD}$  drawn from  $V_{BAT}$ :

$$I_{MAX\_AVG\_VDD} = \frac{P_{OUT}}{V_{DD} \times \eta} = \frac{4.242}{3.8 \times 0.8} A = 1.395 A$$

$$I_{MAX\_PEAK\_VDD} = 2 \times I_{MAX\_AVG\_VDD} = 2 \times 1.395 A = 2.79 A$$

If inductor DCR is 50mΩ, then when the output power of 4.242W, the inductor power loss is:

$$P_{DCR\_LOSS} = 1.5 \cdot I_{MAX\_AVG\_VDD}^2 \cdot DCR = 1.5 \times 1.395^2 \times 0.05 W = 145.9 mW$$

Wherein the coefficient 1.5 is the square of the ratio of the sine wave current RMS value and average value (there is no consideration of the impact of the inductor ripple, the actual DCR loss will be even greater). If the loss which is resulting from DCR is less than 1% at efficiency ( $P_{OUT}=4.242W$ ,  $\eta=80\%$ ), then:

$$I_{AVG\_VDD} = 1.395 A$$

$$DCR = \frac{P_{DCR, LOSS}}{1.5 \cdot I_{AVG\_VDD}^2} \leq 0.01 \times \frac{P_{OUT}}{1.5 \cdot I_{AVG\_VDD}^2 \cdot \eta} = \frac{0.01 \times 4.294}{1.5 \times 1.395^2 \times 0.8} \Omega = 18.3m\Omega$$

According to the working principle of the Boost, we can calculate the size of the inductor current ripple  $\Delta I_L$ :

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f \times L} = \frac{3.8 \times (8.5 - 3.8)}{8.5 \times 1.5 \times 1} A = 1.401 A$$

Thus, the maximum peak inductor current  $I_{L\_PEAK}$  and maximum effective inductor current  $I_{L\_RMS}$  is:

$$I_{L\_PEAK} = I_{MAX\_PEAK\_VDD} + \frac{\Delta I_L}{2} = 2.79 + \frac{1.401}{2} A = 3.491 A$$

$$I_{L\_RMS} = \sqrt{I_{MAX\_PEAK\_VDD}^2 + \frac{\Delta I_L^2}{12}} = \sqrt{2.79^2 + \frac{1.401^2}{12}} A = 2.819 A$$

From the above calculation results:

- 1) For typical DCR about 50mΩ inductance, the efficiency loss caused by around 3%;
- 2) Need to choose the device inductance input current limit value  $I_{LIMIT}$  is greater than  $I_{L\_PEAK} = 3.53 A$  ( $< I_{LIMIT} = 4A$ ), to guarantee the output drive power can be achieved when THD = 1% (= 4.1W) but not limited by value  $I_{LIMIT}$ ;
- 3) In practice, the maximum output power of the drive is likely to reach 4.3W in an instant, so the selected inductor saturation current  $I_{SAT}$  requires more than the maximum inductor peak current  $I_{L\_PEAK}$ , and cannot be less than 3.6A;
- 4) In some cases, if the  $I_{L\_PEAK}$  calculated according to the above method is greater than the set of input inductor current limit value  $I_{LIMIT}$ , shows the output drive is restricted by inductance input current limit, the actual maximum output power is less than the calculated value, the measured value shall prevail, and  $I_{SAT}$  need greater than the set current limiting value  $I_{LIMIT}$ , and cannot be less than 3.6A;
- 5) Take PVDD = 8.5V for example, under different conditions, the typical method of selecting  $I_{SAT}$  in the following table:

VBAT (V)	PVDD (V)	RL (Ω)	ILIMIT (A)	Efficiency(η) (%)	Vp (V)	IL_PEAK (note1) (A)	Inductor saturation current ISAT minimum value (A)
3.8	8.5	8	4	80	8.19	3.53	3.6
3.6	8.5	8	4	80	8.19	3.67	4.0

Note 1:  $I_{L\_PEAK}$  is in parentheses in the "note 1" for power and actual efficiency calculated, if its value is greater than  $I_{LIMIT}$ , then triggers the inductance input current limit.

- 6) Inductor Selection example: Sunlord WPN252012H1R0MT inductance. The inductor package size is 252012, inductance value is 1μH, DCR Typical value is 48mΩ, the typical saturation current  $I_{SAT}$  is 4.2A, the typical temperature rise current  $I_{RMS}$  is 3.4A, suitable for VBAT=3.6V, PVDD=8.5 V, the load impedance  $R_L=8\Omega$ , inductor input current limit  $I_{LIMIT}=4A$ . If you choose  $I_{SAT}$  or  $I_{RMS}$  of the inductance is too small, it is possible to cause the chip don't work properly, or the temperature of the inductance is too high.



Model	Inductance value	producer	size	DCR ( $\Omega$ )	I <sub>SAT</sub> (A)	I <sub>RMS</sub> (A)
WPN252012H1R0MT	1 $\mu$ H	Sunlord	2.5×2.0×1.2mm	0.054	4.2	3.4

## CAPACITORS SELECTION

### Boost Capacitor Selection

Boost output capacitor is usually within the range 0.1 $\mu$ F~47 $\mu$ F. It needs to use Class II type (EIA) multilayer ceramic capacitors (MLCC). Its internal dielectric is ferroelectric material (typically BaTiO<sub>3</sub>), a high the dielectric constant in order to achieve smaller size, but at the same Class II type (EIA) multilayer ceramic capacitors has poor temperature stability and voltage stability as compared to the Class I type (EIA) capacitance. Capacitor is selected based on the requirements of temperature stability and voltage stability, considering the capacitance material, capacitor voltage, and capacitor size and capacitance values.

#### A) Temperature Stability

Class II capacitance have different temperature stability in different materials, usually choose X5R type in order to ensure enough temperature stability, and X7R type capacitance has better properties, the price is relatively more expensive; X5R capacitance change within  $\pm 15\%$  in temperature range of -55°C to 85°C, X7R capacitance change within  $\pm 15\%$  in temperature range of -55°C~125°C. The Boost output capacitance of the device recommends X5R ceramic capacitors.

#### B) Voltage Stability

Class II type capacitor has poor voltage stability Capacitance values falling fast along with the DC bias voltage applied across the capacitor increasing. The rate of decline is related to capacitance material, capacitors rated voltage, capacitance volume. Take for TDK C series X5R for example, its pressure voltage value is 16V or 25V; the package size is 0805, 1206 or 0603, the capacitance value is 10 $\mu$ F. The capacitor's voltage stability of different types of capacitor is as shown below:

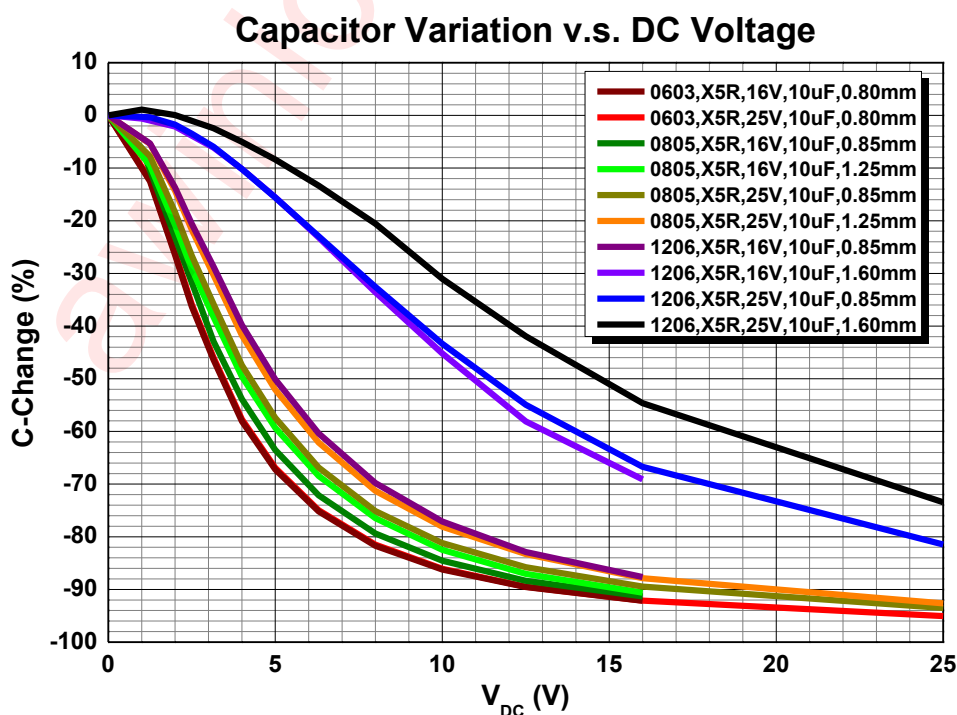
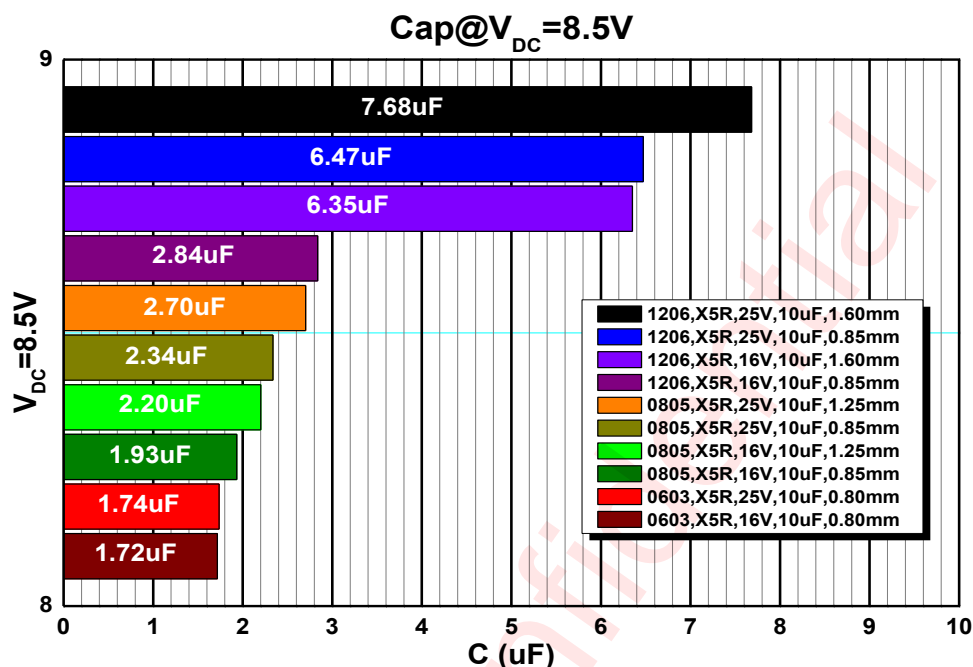


Figure 24 Different Types of Capacitive Voltage Stability

Among them, the space remaining value of different types of capacitors at  $V_{DC} = 8.5\text{ V}$  as shown in the Figure 25:

Figure 25 The Space Remaining Value of Different Types Of Capacitors At  $V_{DC} = 8.5\text{ V}$ 

It can be found that the rate of capacitance capacity value descent becomes slow along with "large capacitor size, capacitance pressure voltage rise". The larger the package size, the better voltage stability. The higher the height, the better voltage stability with the same length and width of the capacitance. Voltage stability of smaller package size (0603) capacitor change affected by the pressure value is very small.

In AW8697 typical applications, it is necessary to ensure the output value of the Boost capacitor  $\geq 5\mu\text{F}$  when  $PVDD=8.5\text{V}$ .

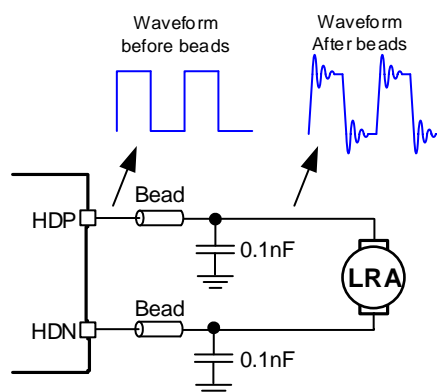
### Supply Decoupling Capacitor ( $C_s$ )

The device is a high voltage driver that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically  $0.1\mu\text{F}$ . This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the device is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the  $0.1\mu\text{F}$  ceramic capacitor, place a  $10\mu\text{F}$  capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

### Output Beads, Capacitors

The device passed FCC and CE radiated emissions with no ferrite chip beads and capacitors. Use ferrite chip beads and capacitors if device near the EMI sensitive circuits and/or there are long leads from driver to load, placed as close as possible to the output pin.

The device output is a square wave signal, which causing switch current at the output capacitor, increasing static power consumption, and therefore output capacitor should not be too large,  $0.1\text{nF}$  ceramic capacitors is recommended.



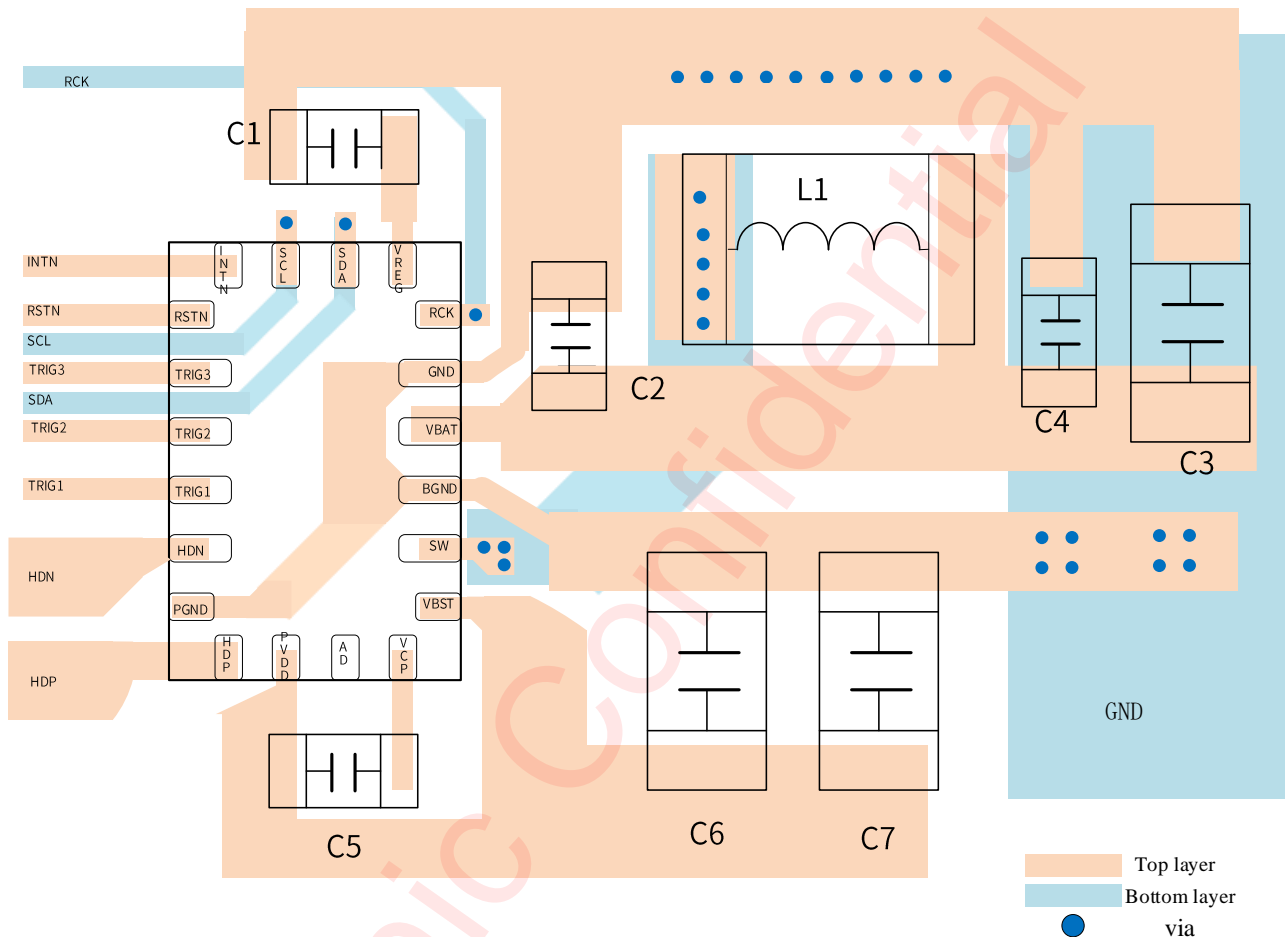
**Figure 26 Ferrite Chip Bead and Capacitor**

The device output is a square wave signal. The voltage across the capacitor will be much larger than the PVDD voltage after increasing the bead capacitor. It suggested the use of rated voltage above 16V capacitor. At the same time a square wave signal at the output capacitor switching current form, the static power consumption increases, so the output capacitance should not be too much which is recommended 0.1nF ceramic capacitor rated voltage of 16V. If you want to get better EMI suppression performance, can use 1nF, rated voltage 16V capacitor, but quiescent current will increase.

## PCB LAYOUT CONSIDERATION

### LAYOUT CONSIDERATIONS

This device is a high voltage driver chip. To obtain the optimal performance, PCB layout should be considered carefully. The suggested Layout is illustrated in the following diagram:

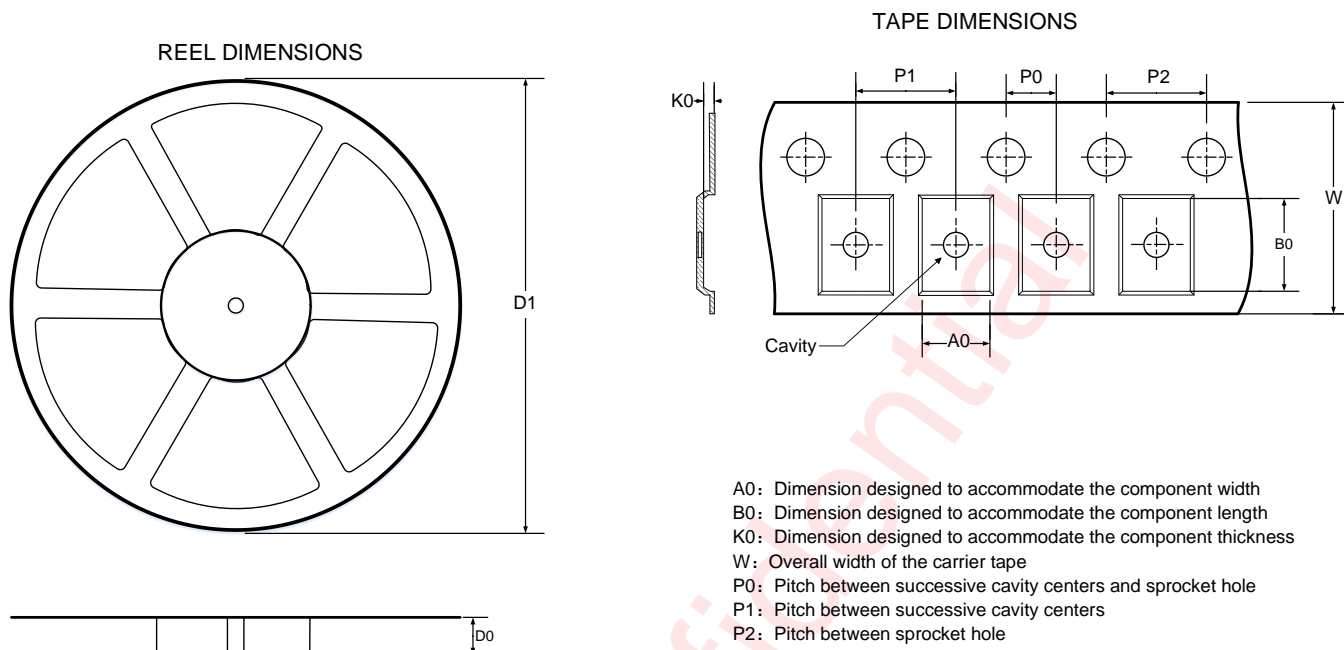


**Figure 27 AW8697 Board Layout**

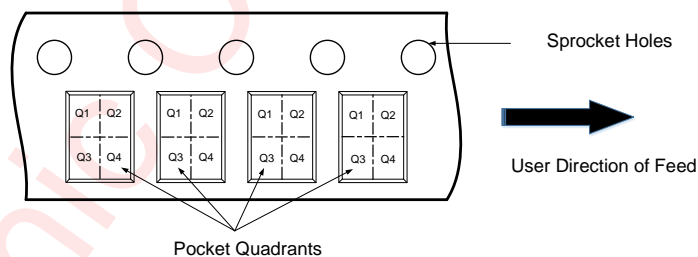
Here are some guidelines:

1. All of the external components close to IC in top layer PCB;
2. No via in traces from IC pin PVDD through C6 to IC pin PGND, keep the trace as short as possible;
3. No via in trace from IC pin VBST through C7 to IC pin BGND, keep the trace as short as possible;
4. Create solid GND plane near and around the IC, connect BGND, PGND and GND together;
5. Try to provide a separate short and thick power line to the device, the copper width is recommended to be larger than 0.75mm. The decoupling capacitors should be placed as close as possible to boost power supply pin;
6. The beads and capacitor should be placed near to the device HDN and HDP pin. The output line from the device to load should be as short and thick as possible. The width is recommended to be larger than 0.5mm;
7. C4, C3 should be placed close to L1.

## TAPE AND REEL INFORMATION



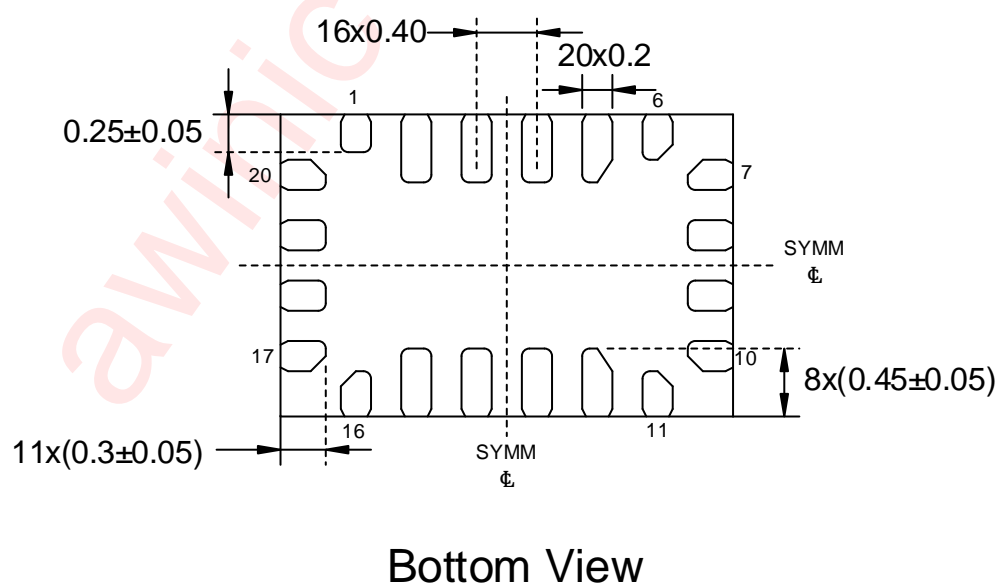
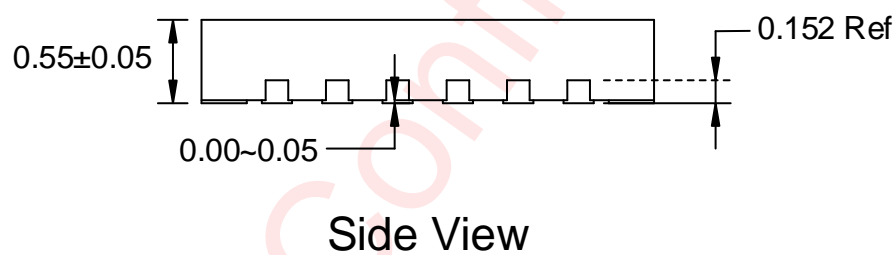
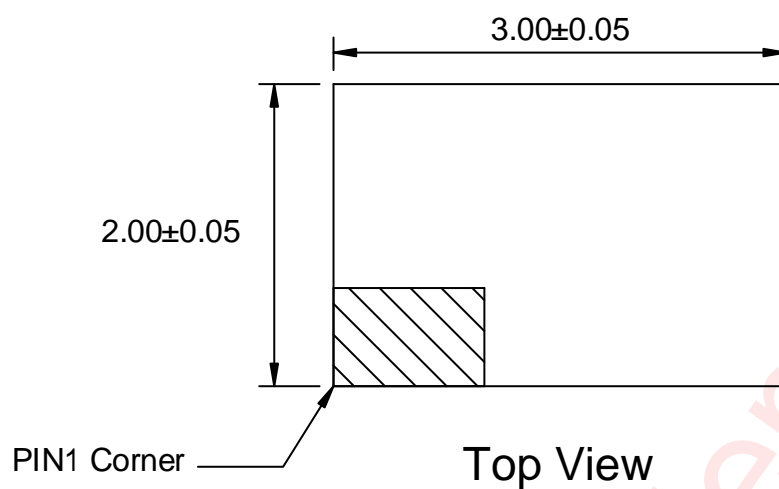
## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All Dimensions are nominal

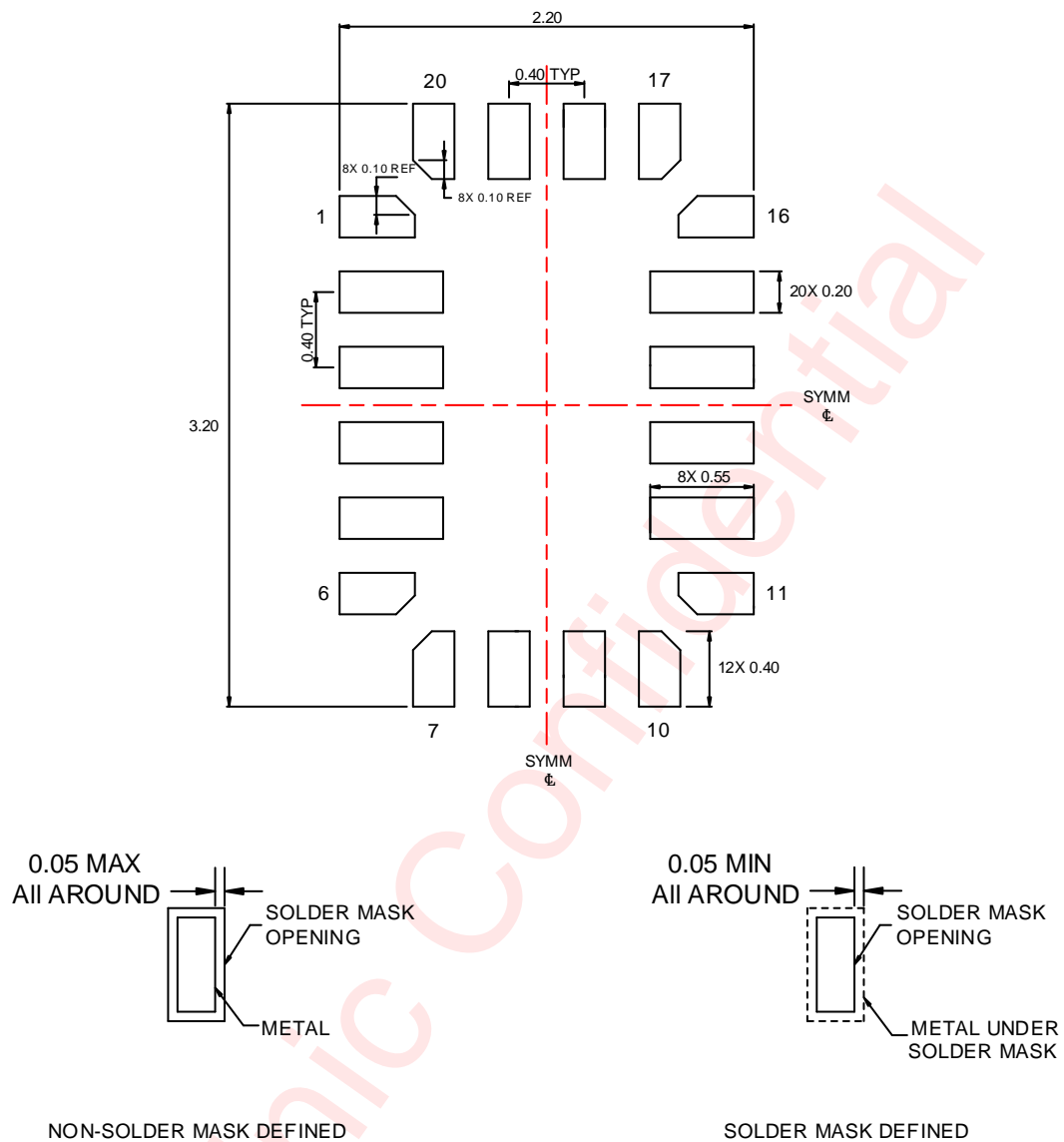
D1: Reel Diameter (mm)	D0: Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	2.3	3.3	0.75	2	4	4	12	Q1

## PACKAGE DESCRIPTION



Unit: mm

## LAND PATTERN DATA



Unit: mm

## REVISION HISTORY

Version	Date	Change Record
V1.0	May 2018	Officially Released
V1.1	August 2018	Add pictures and comments(Figure 8 and Figure 9)
V1.2	August 2018	Modify DVDD to VREG, change CHIPID from 94 to 97
V1.3	October 2018	Modify PVDD configuration, VDD to VBAT and VREG/VCP maximum value
V1.4	October 2018	Update and modify the register list
V1.5	November 2018	Update and modify the register list, update Figure 8 Long Vibration with Automatic Braking
V1.6	January 2019	Update title and application description, update figure of function block diagram and typical application circuits
V1.7	March 2019	Add power on sequence figure
V1.8	September 2019	Tuning some tables and figures
V1.9	November 2019	Change the standby current from 10 $\mu$ A to 8 $\mu$ A Change the I <sub>maxout</sub> from 0.6A to 1A,PVDD=8.5V
V2.0	May 2020	Add power down sequence Correct Figure number errors Change the ESD data
V2.1	August 2020	Change the Figure 10 Delete the maximum output current
V2.2	July 2021	Revise WAIT SLOT register description Revise PCB Layout Consideration



## DISCLAIMER

Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.