Application Note: SY7088

2.3V Minimum Input and 5.5V Maximum Output 3A Peak Current Synchronous Boost with Output Disconnect

Preliminary Specification

General Description

SY7088 is a high efficiency synchronous boost regulator that converts up to 5.5V output voltage. It adopts NMOS for the main switch and PMOS for the synchronous switch. It can disconnect the output from input during the shutdown mode.

Ordering Information

SY7088 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY7088DGC	DFN2x3-8	----

Features

- 2.3-5.0V input voltage range
- Adjustable output voltage from 2.5V to 5.5V
- Pseudo-constant frequency: 1MHz
- 3A peak current limit
- Input under voltage lockout
- Load disconnect during shutdown
- Output over voltage protection
- Low $R_{DS(ON)}$ (main switch/synchronous switch) at 5.0V output: 70/100mohm
- Compact package: DFN2x3-8

Applications

- All Single Cell Li or Dual Cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment.

Typical Applications

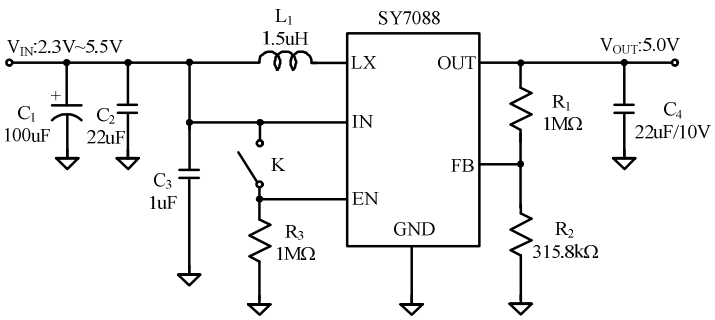


Figure 1. Schematic Diagram

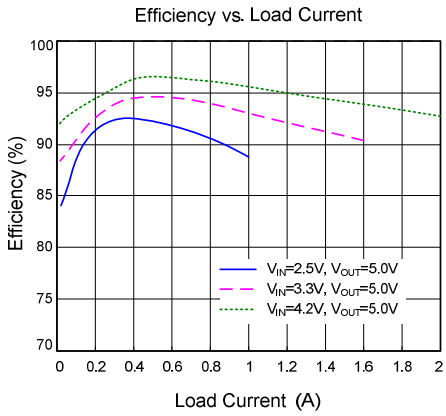
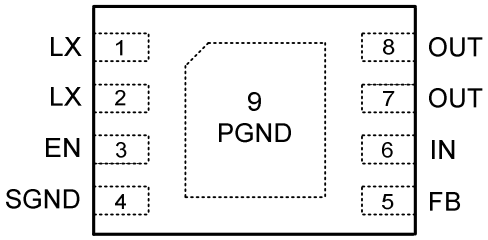


Figure 2. Efficiency Figure

Pinout (top view)



(DFN2x3-8)

Top mark: **VT*xyz*** (Device code: VT, ***x=year code, y=week code, z= lot number code***)

Name	DFN2x3-8	Description
LX	1, 2	Inductor node. Connect an inductor between IN pin and LX pin.
EN	3	Enable pin. Internal integrated with 1Mohm pull down resistor.
SGND	4	Signal ground pin.
FB	5	Feedback pin. Connect a resistor R_H between OUT and FB, and a resistor R_L between FB and GND to program the output voltage. V_{OUT}=1.2V*(R_H/R_L+1).
IN	6	Signal input pin. Decouple this pin to GND pin with at least 1.0uF ceramic cap for noise immunity consideration.
OUT	7, 8	Power output pin. Decouple this pin to GND pin with at least 10uF ceramic cap.
PGND	9	Power ground pin.

Absolute Maximum Ratings (Note 1)

EN---------- V_{OUT}+0.3V
Other Pins---------- 6V
Power Dissipation, P_D@ T_A=25°C DFN2x3-8---------- TBD
Package Thermal Resistance (Note 2)
θ_{JA} ---------- TBD
θ_{JC} ---------- TBD
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN ---------- 2.3V to 5.25V
OUT---------- 2.5V to 5.5V
EN, FB---------- 0V to V_{OUT}+0.3V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =2.4V, V_{OUT}=5V, I_{OUT}=500mA, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		V_{IN}		2.3		5.25	V
Output Voltage Range		V_{OUT}		2.5		5.5	V
Quiescent Current	V_{IN}	I_Q	Io=0A,V_{EN}=V_{IN}=2.3V,		2		μA
	V_{OUT}		V_{OUT}=5.0V		30		μA
Shutdown Current		I_{SHDN}	V_{EN}=0V, V_{IN}=2.4V		0.1	1	μA
Linear charge current		I_{CHARGE}	V_{OUT}<1V		1.2		A
			1V≤V_{OUT}<V_{IN} -0.2V		1.0		
Soft-start time		Tss			0.5		ms
Input Vin UVLO threshold		V_{UVLO}				2.3	V
Vin UVLO hysteresis		V_{hys}			0.1		V
EN Rising Threshold		V_{ENH}		1.2			V
EN Falling Threshold		V_{ENL}				0.4	V
Low Side Main FET R_{ON}		$R_{DS(ON)1}$	V_{OUT}=5.0V		70		mΩ
Synchronous FET R_{ON}		$R_{DS(ON)2}$	V_{OUT}=5.0V		100		mΩ
Main FET Current Limit		I_{LIM}		3			A
Feedback Reference Voltage		V_{REF}		1.182	1.2	1.218	V
Minimum on time		T_{ON_MIN}			100		ns
Max on time		T_{ON_MAX}			2		μs
OUT pin OVP protection		V_{OVP}			6		V
OUT pin OVP hysteresis		V_{OVP_HYS}			0.2		V
Thermal Shutdown Temperature		T_{SD}			150		℃
Thermal Shutdown hysteresis		T_{HYS}			20		℃

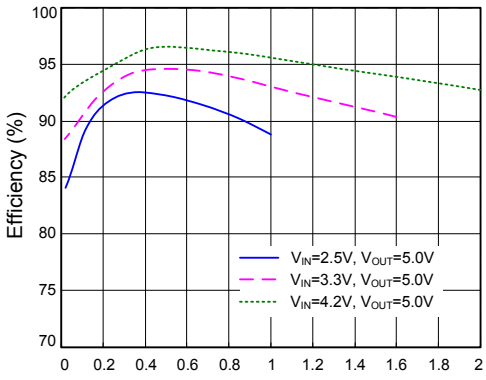
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θJA is measured in the natural convection at T_A = 25°C on a two-layer Silergy Evaluation Board..

Note 3: The device is not guaranteed to function outside its operating conditions.

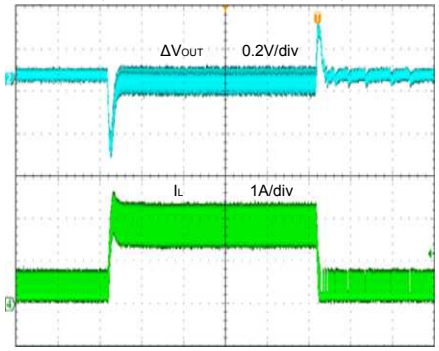
Typical Performance Characteristics

Efficiency vs. Load Current



Load Transient

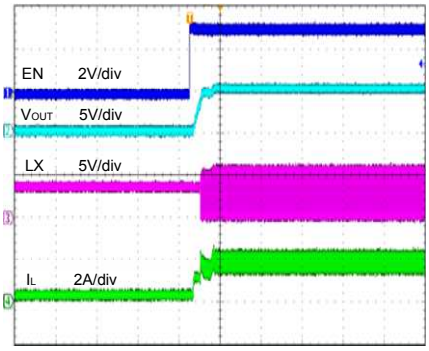
(V_{IN}=3.3V, V_{OUT}=5.0V, I_O=0.1- 1.0A)



Time (200μs/div)

Startup from Enable

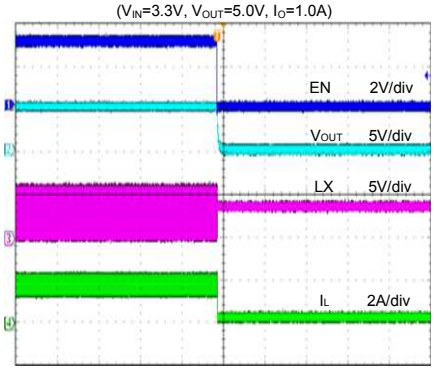
(V_{IN}=3.3V, V_{OUT}=5.0V, I_O=1.0A)



Time (800μs/div)

Shutdown from Enable

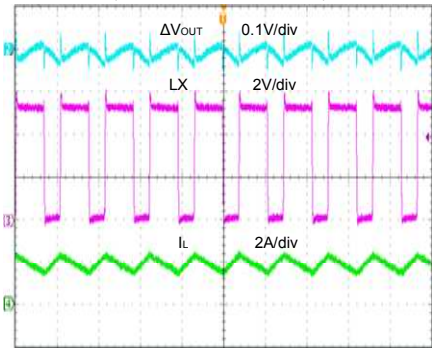
(V_{IN}=3.3V, V_{OUT}=5.0V, I_O=1.0A)



Time (4ms/div)

Output Ripple

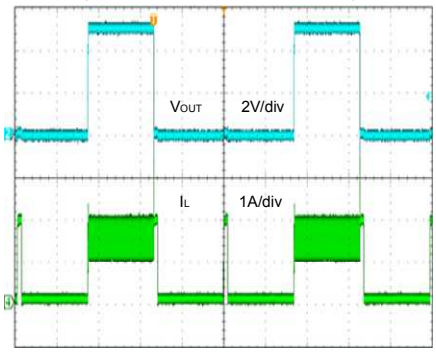
(V_{IN}=3.3V, V_{OUT}=5.0V, I_O=1.0A)



Time (1μs/div)

Short Circuit Protection

(V_{IN}=3.3V, V_{OUT}=5.0V, I_O=1.0A to Short)



Time (20ms/div)

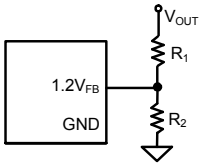
Applications Information

Because of the high integration for SY7088, only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R1 and R2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is recommended for both resistors. If V_{OUT} is 5.0V, R_1=470kΩ is chosen, using following equation, then R_2 can be calculated to be 148.4kΩ:

$$R_2 = \frac{1.2V}{V_{OUT} - 1.2V} R_1$$



Input capacitor CIN:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins. In this case, a 22uF low ESR ceramic capacitor is recommended.

Output capacitor COUT:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 10V rating and greater than 22uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = (\frac{V_{IN}}{V_{OUT}})^2 \frac{(V_{OUT} - V_{IN})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY7088 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,MAX} + \frac{V_{IN}}{V_{OUT}} \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mohm to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY7088 shutdown current drops to lower than 1uA, Driving the EN pin high (> 1.2V) will turn on the IC again.

Layout Design:

To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{SIN}, C_{OUT}, L, R_H and R_L.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable. PGND and SGND pins are recommended to connect to exposed paddle directly. Reasonable via holes are recommended to be placed under the exposed paddle for the better performance consideration.

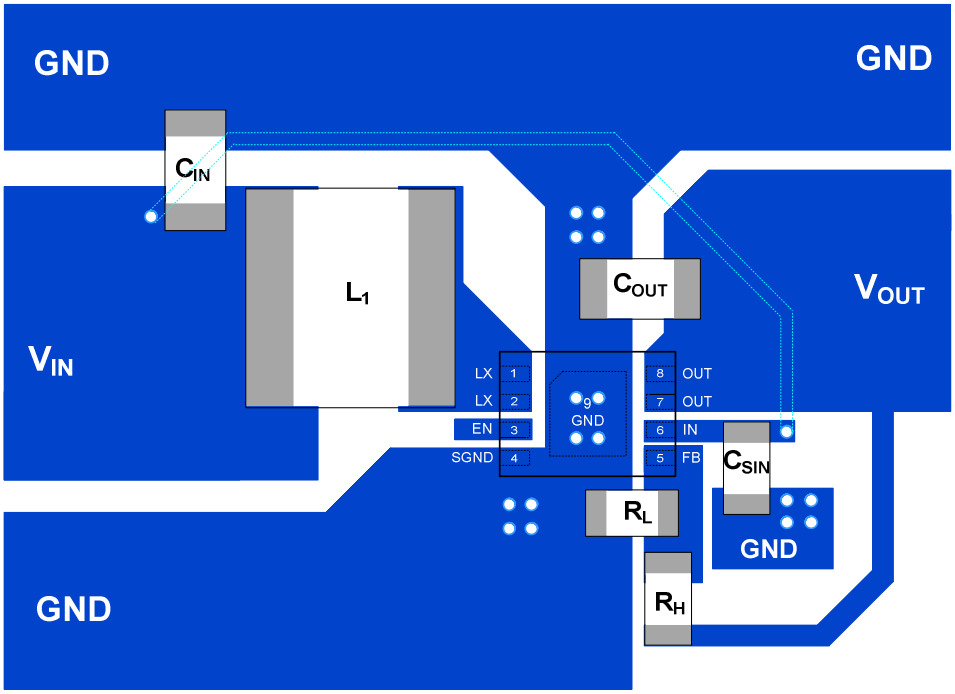
2) For boost converter, the output current is discontinuous. So the loop area formed by C_{OUT}, OUT and PGND must be minimized.

3) The decoupling capacitor of IN to GND C_{SIN} must be placed as close as possible with IN pin.

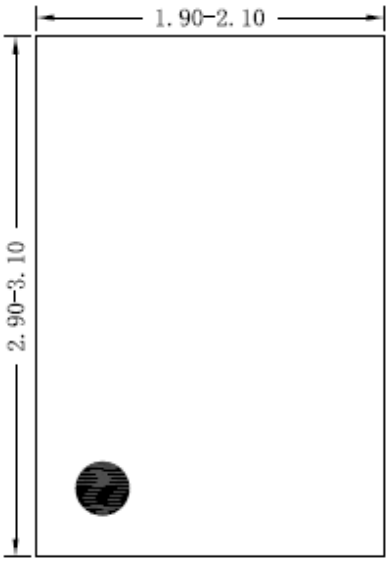
4) The PCB copper area associated with LX pin must be minimized to improve the noise immunity.

5) The components R_H, R_L and the trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to FB pin.

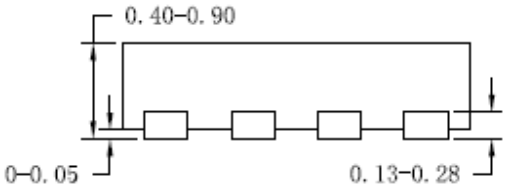
PCB Layout Suggestion



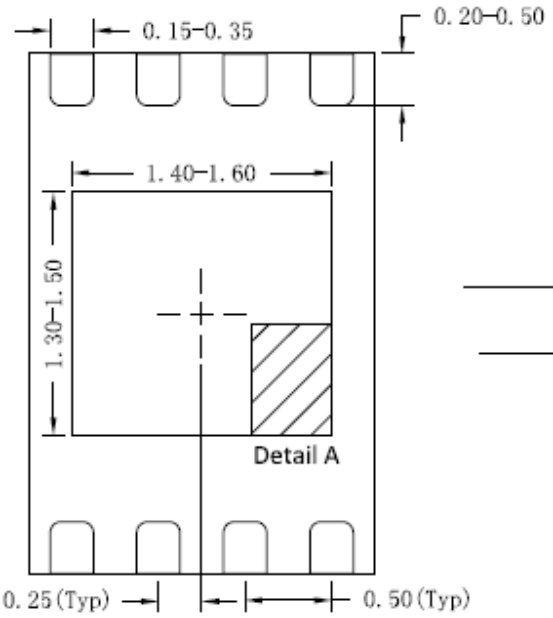
DFN2x3-8 Package Outline

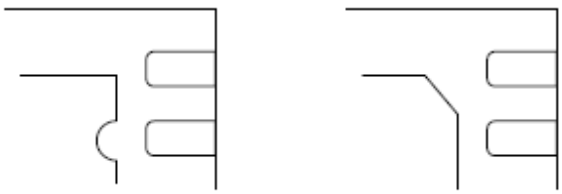


Top View



Side View





Detail A
Pin1 Identifier: two options

Bottom View

Notes: **All dimension in MM and exclude mold flash & metal burr**